A Novel Topology using Cuk Converter in PV Microconverter with Transformerless Injection

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***Abstract*— The ´Cuk derived inverters, employing second-order input and output filters, offer the most efficient, lightweight, and economical solution in the class. This paper presents design and detailed operation of a ´Cuk derived, common- ground PV microinverter in continuous conduction mode operation. The inverter is shown to be compatible with both linear and nonlinear loads, in stand-alone and grid- connected modes of operation. Optimal design rules of passive components are rigorously derived to ensure attenuation of input voltage ripples arising from the twin effects of switching and double-frequency output power oscillation.**

Index Terms*— Common grounding, inductor design, photovoltaic (PV) inverter, single-stage inverter, transformer-less inverter.

I. INTRODUCTION

POTENTIAL induced degradation of solar photovoltaic (PV) modules is caused by ground leakage current [1], which reduces module power capacity. Leakage current occurs due to common mode voltage (Vcm), defined as [2], [3]

$$Vcm = (Van + Vbn)/2 \qquad (1)$$

in an H-bridge inverter (see Fig. 1). While using unipolar pulse width modulation (PWM), Vcm varies at inverter switching frequency and its multiples. The low impedance offered by the parasitic capacitance (Cpv), between earth and PV, at these frequencies causes large common mode currents[2],[3].Reduction in the common-mode frequency has been achieved using bipolar

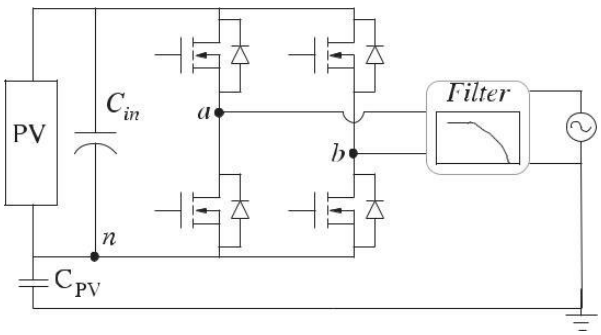

Fig. 1. Leakage current in H-bridge inverter.

PWM [4] or multilevel, neutral-point clamped transformerless topologies [4], [5], or its variant using split inductors [4], [6], [7]. But these offer no voltage boost and hence require series connection of a large number of PV panel so raprior boost stage, both of which degrade the efficiency. H-bridge derived topologies, viz., H-5, H-6, HERIC [8] and HB-ZVR inverters [9] decouple the PV modules from the grid during current freewheeling, when the PV terminals are left floating. For such PV systems, NEC 690.35 stipulates additional ground fault protection. Since the utility neutral is al-ready earthed, this additional protection is inherently obviated in common-grounded PV interface. Though a line-frequency transformer easily achieves double grounding, it makes the system bulky. Topologies using high-frequency transformers [10], [11] suffer from increased losses in the ensuing three-stage power conversion.

II .EXISTING SYSTEM

Several common-grounded, transformerless topologies have been reported in the literature [12]–[23], which implicitly com- bine buck–boost and inversion functions. Of these [12], a buck– boost derived topology comprises five active switches and two diodes. In every half cycle, the inductor connections with respect to the output capacitor are reversed by a switch network. A variant [13], based on the same principle, uses an extra diode. However, both are unable to transact reactive power because the series diodes prevent current reversal. Using a pair of coupled inductors, [14] proposes a combination of ´Cuk and Watkins–Johnson topologies. However, this results in higher currents in the coupled windings, which increases both inductor size and losses. In [15], the circuit topology alternates between a ´Cuk converter, during the negative half cycle of the output ac volt- age, and Zeta converter, for the positive half. Since the plant model changes every half cycle, controller design becomes exceedingly complex.

III. PROPOSED SYSTEM

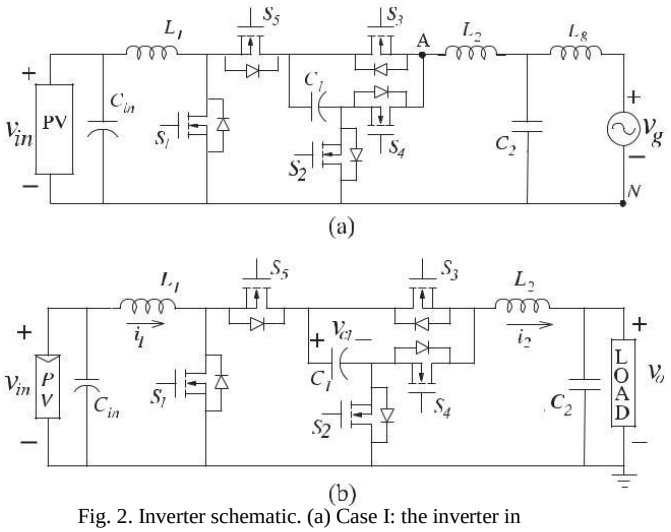

Fig. 2. Inverter schematic. (a) Case I: the inverter in GC mode. (b) Case II: the inverter in SA mode.

An interesting ´Cuk derived topology [16] achieves cyclic reversal of the connection between the intermediate dc-link capacitor and the output filter, during each half cycle of the output ac voltage. Plant models in the two modes, corresponding to positive and negative output voltages, are similar [24]. Since the inverter retains all the advantages of a ´Cuk converter, in terms of efficiency, weight and cost [25], it is the better solution in the class. Another variant [17] uses an extra switch in the free- wheeling path of the output filter to reduce conduction loss. In both [16] and [17], use of diodes in series with switches pre- vent load and source current reversal within each of the modes. Also, the switching sequence is only applicable for unity power factor (UPF) loads, which unnecessarily limits the scope of this promising circuit topology. The major lacuna, however, is in the lack of any justifiable basis for the major performance metrics and design equations which, on some occasions, lead to unacceptable inaccuracies. No analytical or experimental validation of the design rules, for the passive components in the circuit, is provided. This paper presents a modification in the topology of [16], [17], which allows bidirectional power flow, hence enabling applications involving reactive loads, in addition to UPF loads. It thus includes a thoroughly different switching strategy, apart from justified circuit design rules. Operation of the proposed converter is presented in Section II, where steady-state expressions for inverter states and voltage gain are derived for ideal and nonideal circuit elements. Section III analyzes the effect of double-frequency power oscillation on the input voltage. Section IV systematically lays down well-justified and vastly improved design rules for the inverter components. All analytical conclusions are experimentally validated with a 300-VA laboratory prototype.

IV. CIRCUIT DESCRIPTION AND OPERATION

Circuit diagrams of the inverter in grid connection (GC) and stand-alone(SA)modes are shown in Fig.2.The circuit does not require any common-mode noise filter. The negative conductor
and grid neutral (N) are shorted to ensure common grounding hence reduced or no common mode ground current.In GC mode of operation earth connection is provided through grid neutral, whereas in SA mode then egative railisear thed to avoid runaway potential at the circuit nodes. Composition of circuit elements includes one dc capacitor (C1), five MOSFET (two quadrant) switches (S1 −S5) and second-order input (Cin,L1) and output (C2,L2) filters. Switch S1 is considered as the main switch and the time interval when switch S1 is ON is designated as ON time, the remaining duration of the switching period is designated as OFF time. Depending upon output voltage polarity the inverter operates in two modes, as described below. For ease of explanation, the PV source is replaced by a dc voltage source, Vin.

A. Mode-1 (Vo > 0)

Fig. 3(a) and (b), respectively, show the circuit configurations for the ON and OFF times in this mode of operation. Reference capacitor voltage polarities and inductor current directions are

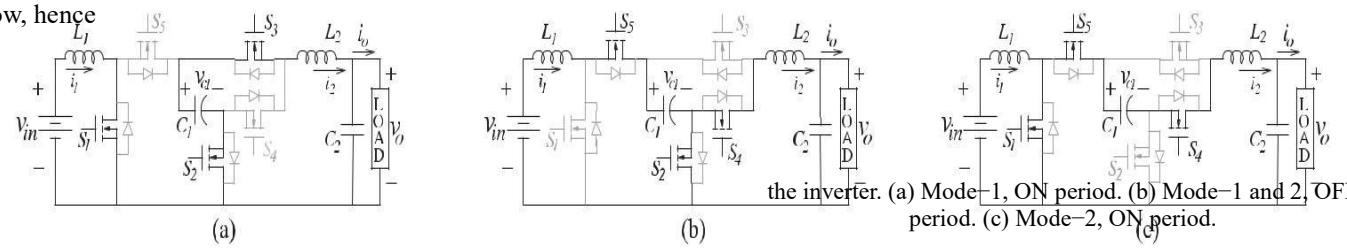

Fig. 3. Circuit diagrams during various operating states of the inverter. (a) Mode−1, ON period. (b) Mode−1 and 2, OFF period. (c) Mode−2, ON period.

indicated. The actual inductor current direction depends upon the load. Switch current (iS1,...,iS5), inductor current and capacitor voltage waveforms with switching signals, Sg1,...,Sg5 of devices S1,...,S5 respectively, are shown in Fig. 4(a). Since MOSFETs allow bidirectional current flow, the inverter operates in continuous conduction mode under all the load conditions. Considering flux-balance of inductors L1 and L2, steady-state duty cycle average (DCASS) [26] of vc1 and vo, over one switching period Ts are obtained as

$$V_{c1}^{(1)} = V_{in} + V_0^{(1)} \qquad (2)$$

where D is the steady-state duty cycle. Equating input and output powers, and using (3), DCASS of i_1 is expressed as

$I_1^{(1)} = (V_0^{(1)} / V_{in})$ $I_0 = (D/1\text{-}D)\, I_0$

$\Delta i_1 = (Vin\ DTs)/L1$ (5)

$\Delta v_{c1} = \{| I_1^{(1)} | (1-D)Ts\}/C1 = (|Io|DTs) / C1$ (6)

$\Delta i_2 = \{ V_0^{(1)} (1-D)Ts\}/L2 = (Vin\ DTs) / L2$ (7)

Currents passing through switch pairs (S1,S5) and (S3,S4) are i1 and i2, respectively. During ON period current through S2 is i2, whereas during OFF period this is (i1 −i2). Switches S1 and S3 −S5 are required to block a forward voltage of magnitude equal to|vc1|. Energy transfer during ON and OFF times depends upon load current direction. Thus two cases are formed, which are as follows.

1)Case-1a, (Io > 0): This is the forward powering mode. Inductor current directions are as shown in Fig. 3(a) and (b).

2)Case-1b, (Io < 0): This is the forward braking mode, which is relevant for reactive loads. Inductor current directions are opposite to those shown in Fig. 3(a) and (b).

B. Mode-2, (Vo < 0)

Fig. 3(b) and (c) show the circuit configurations for this mode during OFF and ON times, respectively. Switching waveforms of capacitor voltage,inductor current,and switch current are shown in Fig. 4(b). In this mode, S1 and S2 are switched in a complementary manner. Also, throughout the switching period, both S4 and S5 are kept in conduction while S3 is not triggered at all. Assuming switching ripples on the states are small, expressions for DCASS of vo and vc1 are

$V_0^{(2)} = -V_{in} (D / 1\text{-}D)$ (8)

$V_{c1}^{(2)} = (V_{in} / 1\text{-}D) = V_{in} - V_0^{(2)}$ (9)

Current i1 and switching ripple in states (Δi1, Δvc1,Δ i2) are expressed by (4)–(7), which were derived for Mode 1 operation. Currents passing through switch pair (S1,S2) is (i1 −i2) and that through S4 is i2. Switch S5 carries i2 and i1 during ON and OFF periods, respectively. The forward blocking voltages of S1, S2, and S3 are identically equal to the magnitude of vc1. The two cases for different directions of load current are as follows.

1)Case-2a (Io < 0): This is the reverse powering mode and inductor current directions are as shown in Fig. 3(b) and (c).

2) Case-2b (Io > 0): This is the reverse braking mode and arises while feeding reactive loads. Inductor current directions are opposite to those shown in Fig. 3(b) and (c).

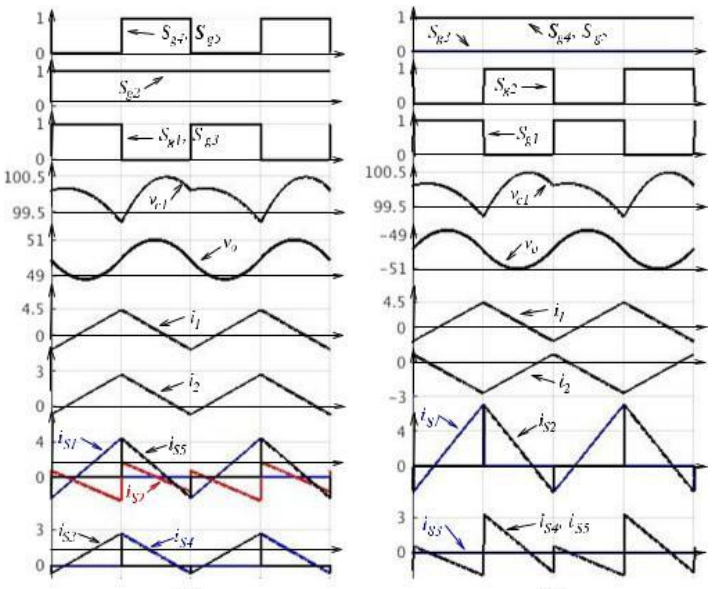

Fig. 4. Switching signals, inductor current,switch current, and capacitor voltage waveforms. (a) Mode−1. (b) Mode−2.

TABLE I
ON–OFF STATES OF SWITCHES

Switching signal	Mode-1, M=1		Mode-2 , M=0	
	On period	Off period	On period	Off period
Sg = Sg 1	1	0	1	0
Sg 2	1	1	0	1
Sg 3	1	0	0	0
Sg 4 , Sg 5	0	1	1	1

C. Design of Inductor L1 and L2

Design constraints for L1 and L2 are first individually specified. Subsequently, details of engineering optimization to minimize losses are presented.

1) Constraints for L1: L1 is required to ensure the switching ripple in vin is restricted to the allowable maximum, ΔV (s) in .

$\Delta V_{in}^{(s)} \geq (1/2C_{in})\ (\Delta i_1/2)\ (T_s/2)$ (10)

$L_1 \geq L^{(1)}_{1,min} = Vin\ DT^2s / (8Cin\ \Delta V_{in}^{(s)})$ (11)

$L_1 \geq L^{(2)}_{2,min} = V_{in} D_{max} T_s / \Delta i_{1,max}$
$(V_{in} T_s / \Delta i_{2,max})\ (V_m / V_m + V_{in})$ (12)

2)Constraint for L2: Minimum value of L2 is decided by the maximum allowable switching current ripple. Using (7), and (10)

$L_2 \geq L_{2,min} = V_{in} D_{max} T_s / \Delta i_{2,max}$

$(V_{in} T_s / \Delta i_{2,max})\ (V_m / V_m + V_{in})$ (13)

TABLE II
SWITCH RATINGS

Parameters	S1 ,S2	S3 ,S4	S5
Current	Im {1+(vm /vin)}	Im	Im (vm /vin)
Voltage	Vm + vin	Vm + vin	Vm + vin

E. Selection of Switches

Minimal switch rating is obviously based on the maximum on-state current and off-state voltage, which are detailed in Section-II. Based on this, Table III lists the selection criteria for all the converter switches.

TABLE III
SYSTEM PARAMETERS

Inverter Rating	Input 40-100 V dc Output 300VA,110 V
Switching frequency fs	50kHz
L_1 and r_1	52 µH, 2 mΩ
$L_{2\ and}$ r_2	120 µH, 7 mΩ
C_1 and ESR	11 µF, 8 mΩ
C_2 and ESR	3.8 µF, 21 mΩ
C_{in} and ESR	2.2 mF, 65 mΩ
r_s	100 mΩ
S1 ,S 2 ,S 5 (S3 ,S 4)	IRFP4868 (FDA38N30)

V.SIMULATION AND RESULT

a)Mode-1 ON Period

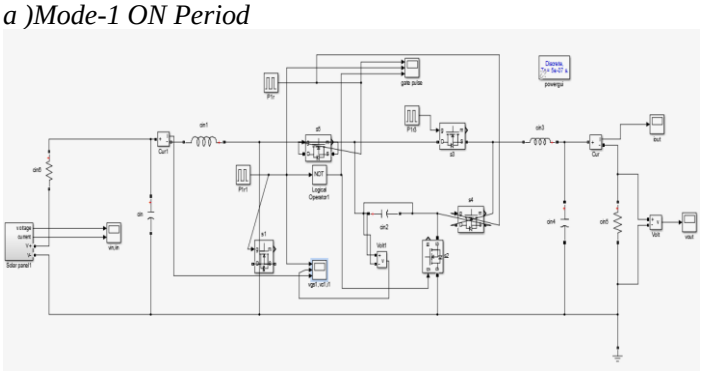

Fig 5. Simulation diagram of mode-1 ON period

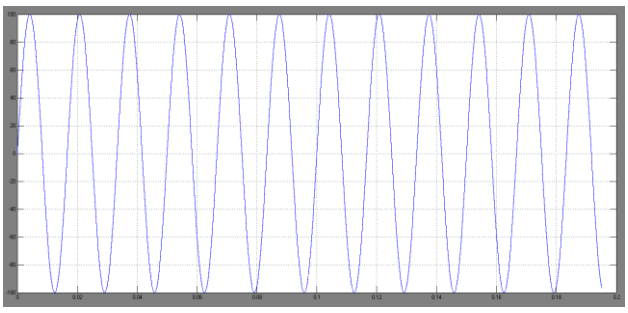

Fig 6. Vout

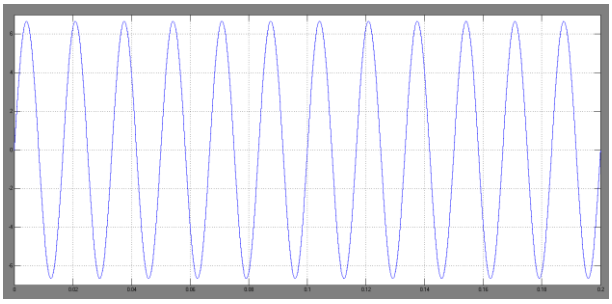

Fig 7. Iout

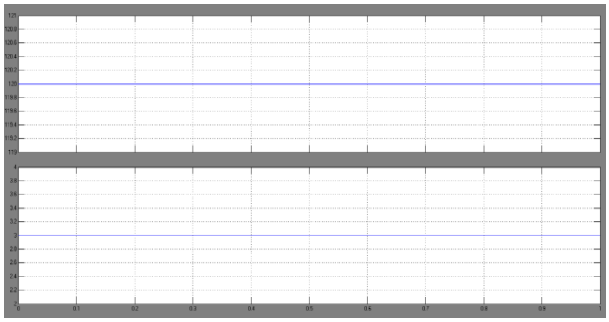

Fig8. Vin Iin

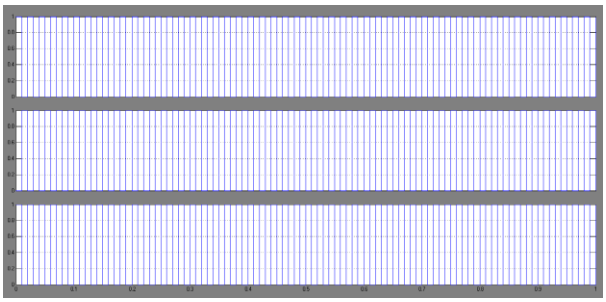

Fig 8.Gate pulse

b) Mode-1, And Mode 2 Off Period

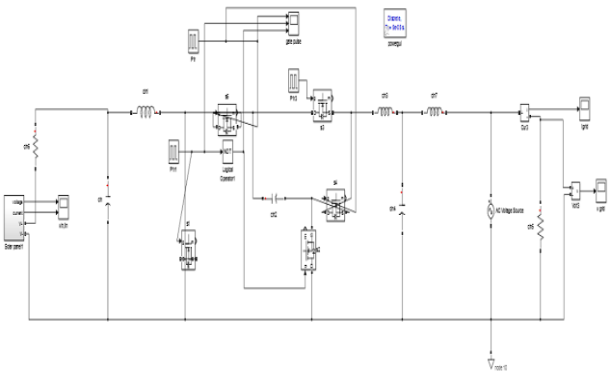

Fig9.Simulation Diagram Of Mode-1 And Mode-2 Off Period

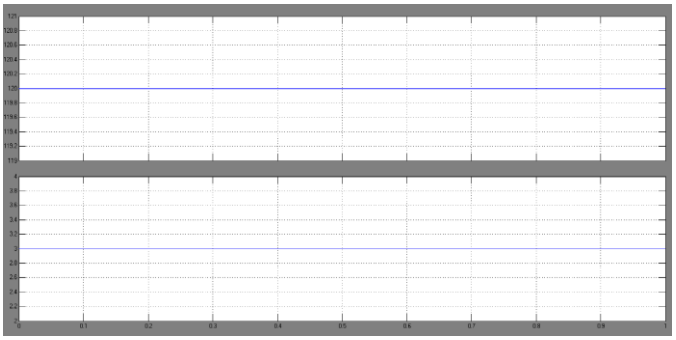

Fig 10. Vin I in

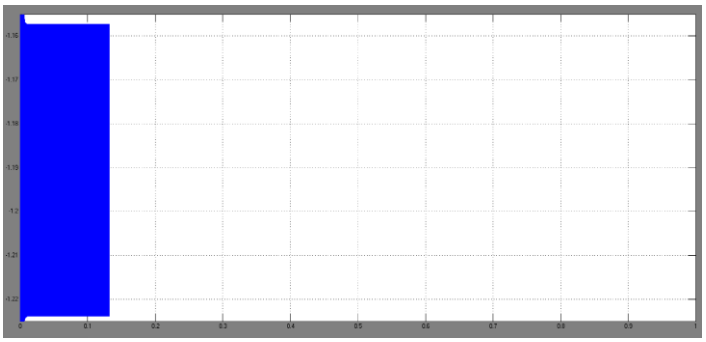

Fig 10. I out

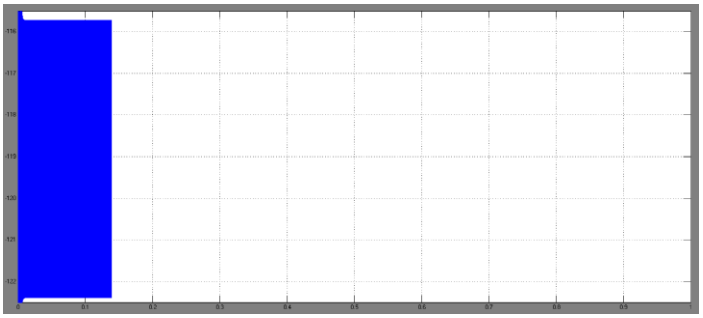

Fig 11. V out

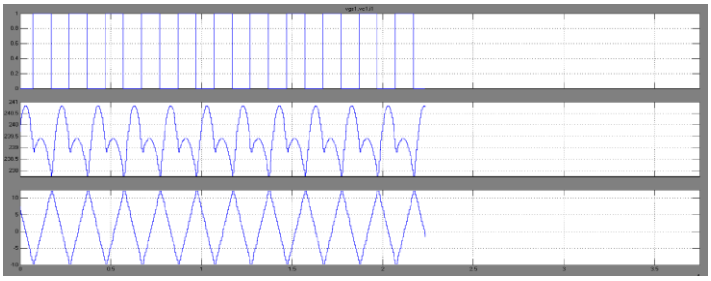

Fig 12. Gate pulse

C) Mode-2 ON period

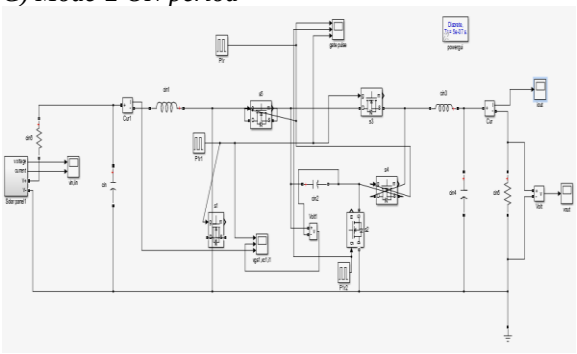

Fig13.simulation diagram of mode-2 ON period

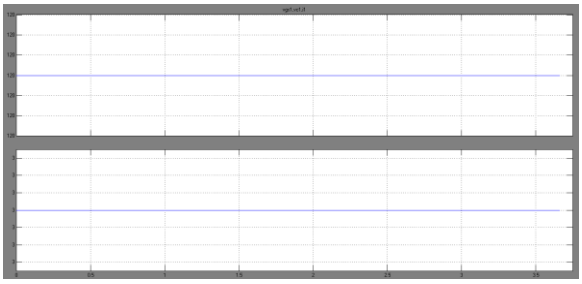

Fig 13.Vin ,Iin

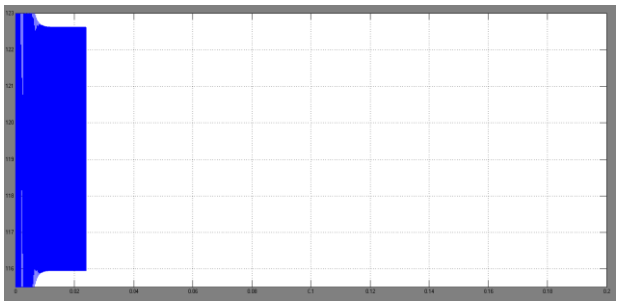

Fig14. V out

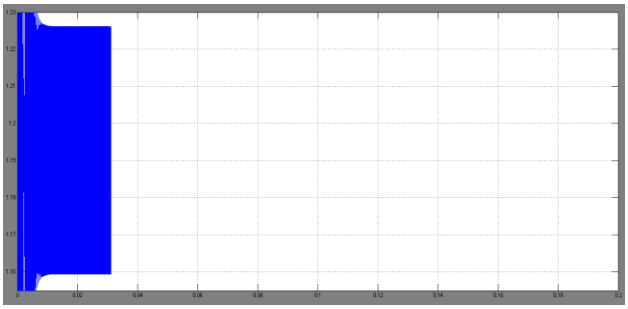

Fig16. I out

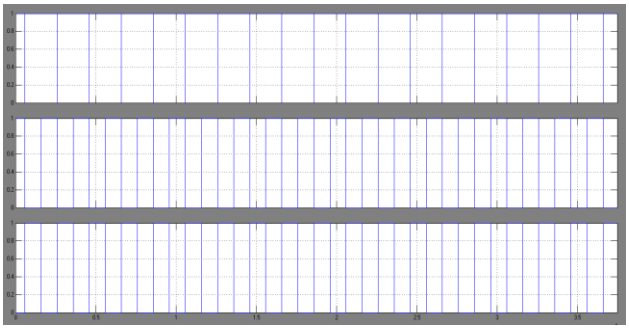

Fig17. Gate pulse

VI. CONCLUSION

This paper presented the design, operation, and performance of a cost effective, compact, nonisolated, single-stage, single- phase dc–ac PV interface. The topology was specifically de- signed to practically eliminate common-mode ground leakage current, which has been validated experimentally. All the operating modes, including dead-time operation, were detailed. Optimal design of passive components was described, which consider ripple components due to both switching and double- frequency power oscillations. Additionally, design of all induc- tors was aimed at maximizing overall efficiency. Output filter design ensured improvement in resonance damping for easing control complexity, while minimally affecting power losses. Inverter performance, with linear/nonlinear loads in SA mode and UPF operation in grid-connected mode, was verified by experiment. Output voltage THD in SA operation and output current.

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