A Novel High Efficient Six Stage Charge Pump based PLL

Ms. Monica.B.J.C (Student)
Department of ECE (Applied Electronics),
Dhanalakshmi Srinivasan college of Engineering,
Coimbatore, India.

Ms. Yamuna.J (Assistant Professor),
Department of ECE,
Dhanalakshmi Srinivasan college of Engineering,
Coimbatore, India.

*Abstract:-*CMOS is used to construct the integrated circuits with low level of static leakage. With this low level leakage we are designing all the transistor circuits in CMOS logic. To control this static leakage in the circuits the supply voltage is a major concern. Here a six stage charge pump with control scheme to reduce threshold voltage is analyzed. These control schemes include body bias effect and backward control scheme. The backward control is to be processed for control the internal voltage when the charge transfer switch could be in activation.

When the supply voltage is to be raise from the fixed voltage level it will be turn OFF the transistor. The maximum level of the converters circuits contain the branch A and branch B which could be contains all p-MOS and n-MOS combinations. The six stage charge pump is employed for Phase locked loop (PLL) application and its performance is analysed. Inorder to further improve the performance, a suitable phase detector and oscillator is predicted for this six stage CP based PLL. These circuits are to be designed and verified by using the TANNER T-SPICE TOOLS.

Key points: - Low power, Charge pump, Phase locked loop, Body bias.

I. INTRODUCTION

A charge pump circuit provides a voltage or a voltage of reverse polarity to upgrade the [2] amplification process. In several applications like Power IC, continuous time filters, and EEPROM, voltages [3] on top of the facility provides square measure often times needed. Redoubled voltage levels square measure obtained during a [4] charge pump as a results of transferring charges to a electrical phenomenon load and do not involve amplifiers or transformers [12].

For that reason a charge pump may be a device of alternative in semiconductor technology [10] wherever traditional vary of operative voltages is proscribed. Charge pumps usually operate at high frequency level so as to [5] extend their output power among an inexpensive size of total capacitance used for charge transfer. This operative frequency is also adjusted by compensating [9] for changes within the power needs and saving the energy delivered to the charge pump.

Among several approaches to the charge pump style, the switched-capacitor circuits like Dickson [4] charge pump square measure very fashionable; as a result of they will be enforced on constant chip together with alternative [8] elements of AN integrated system. The voltage gain of Dickson charge pump is proportional to the amount of

stages within the pump. it should price quite several [11] devices and silicon space, once a charge pump with the voltage gain larger than ten or twenty is required. Such high voltage gains square measure needed for low voltage EEPROMs, and generally quite 3 stages of Dickson charge pumps square measure used. Improved Dickson charge pumps for low voltage EEPROMs and flash recollections [9] square measure developed. Charge pump operates by shift ON and OFF an oversized range of MOS switches that charge and discharge an oversized range of capacitances, [13] transferring energy to the output load.

The required voltage level conversion and the amplification of the charge pump give the [5] better output and easily implemented in the all implementations. The devices that could be effort based on the all level of processing in the various that could be considered for [8] the leakage process. The mode of operation also to be varies and it could be provide various levels of operations based on the technology in the linear level of compensation. The most frequency adjustment could be from the 50Hz to the 500MHz. The architecture level conversion into the circuit design of process may or may not be vary from the IC'S [11].

So the designing process could be give the better result such as low power, better noise performance, and also to could not damage the devices [9]. This condition could be satisfied as per the process of all level of variations from the related units of the charge pump circuits. The implementation could be analyzed as per the rules of the charge pump and the phase detector units. This could be implemented into the application [10] of PLL (Phase Locked Loop). This PLL give the frequency synthesizer for power grid applications for energy harvesting. This could be managed as per the elements of the switching activity from the main circuit.

II. EXISTING SYSTEM

The charge pump circuit has to be design in the environment of short circuit current limit and the as well as the temperature protection. This could be used for the further processing of the voltage level of conversion from the circuit based on the all level of conversion of power and the current limit. This is mainly focused for the power grid applications. In existing system there are many charge pump has been designed and having many limitations.

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In Dickson charge pump the respective switches could be given into the circuit that is the possible combination of the n-MOS and the p-MOS. This could be switches as per the number of stages provided in the circuit combination of the charge pump. From the capacitance for charging and discharging units could be considered. In this charge pump circuit the extension could not be possible and cannot be added for the real time process. This could cause various errors during the testing of chips.

Fig.1. Dickson charge pump

In Wu Chang charge pump circuit the substantial uses of the circuit does not mismatch the p-MOS and the n-MOS conditions of the stages. And also this stage requires the more loop filters and also more current sources. Then this stage of the circuit occupies large silicon area of the chip causes more noises. Then charge pump circuit having the clock feed through and also this is not fully eliminating the charge sharing problems.

The Linear charge pump circuit having the limiting output voltage level form the desired area of the circuit conversion from the number of stages. This inverter level coupling stages could be providing amplitude degradation. And also providing switch mismatch condition for the all dead zone. By using this single ended coupling from the stages of all the coupling inverter gives the results for the more number of parasitic capacitance.

The main architecture of this system provides the non-ideal effects in the system. This could be causes more power consumption and could not be used for the implementation of the charge pump units. The required units cannot be adopted for the uses that carry the structural units from the circuit level of implementation process. The various units can be applied for the large stages and it also occupies the more area in the chip. The testing level of process cannot be accessed for the duration of the individual characteristics of the stages performing the operation of the all coupling. The main work could be considered for the process in the application of duration from the transmission gate charge pump structure.

III. SIX STAGE CHARGE PUMP

This charge pump has the six stages and then the coupling of the inverter stages and also for each branch. The body biasing and the backward control scheme has been applied to the each number of coupling stages and also could be provide the node level of separation from the each stages. The inverter coupling could be processed under the technology that could be beyond the network based applications.

The each node of operation having the reverse biasing voltages and also could be processed for the more stages form the applications. This charge pump has been used for the real time implementation of the Phase Locked Loop. This is the feedback combining system for the linear process that could be connected to the phase detector and the voltage controlled oscillator for the process of all variations from the units. This could be fixed the low frequency signal for the extension of the phase variations from the two input signals.

The six stage charge pump circuit has been shown in Fig 2. The stages of inverter coupling have been adopted from the four level of inverter. This could be connected to the each branch of the circuits for the linear operation of the six stages of the proposed charge pump. The inverter coupling and also the capacitance (1pF) of the 1st stage of the two branches has been given to the input voltage supply.
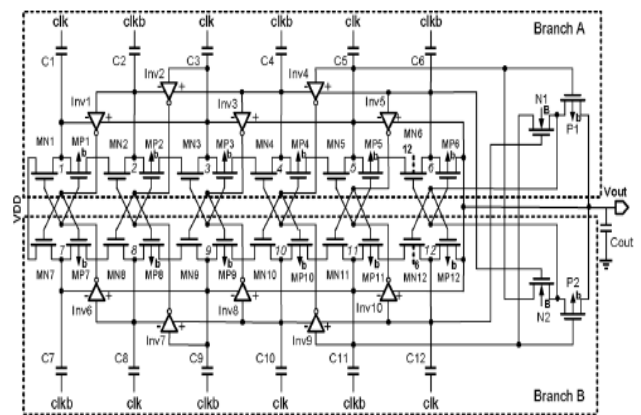

Fig.2. Six stage Charge pump with inverter stages

The capacitors from c1 to c6 in the two branches are used for the charging and discharging of the energy consumption based technique and also used for the amplification of the input voltage from the each stages. Then the body biasing can be applied from the node 1 of the c1 and the MN1 coupling with the MP1. This could be transferred to the branch B of the capacitance node 7 of c1. The coupling of the MN7 and the MP7 (Fig 3) of branch B gives the amplitude stage of first level voltage from the capacitor. The clock frequency has to be given into the circuit combination from the clk and clkb to the two branches.
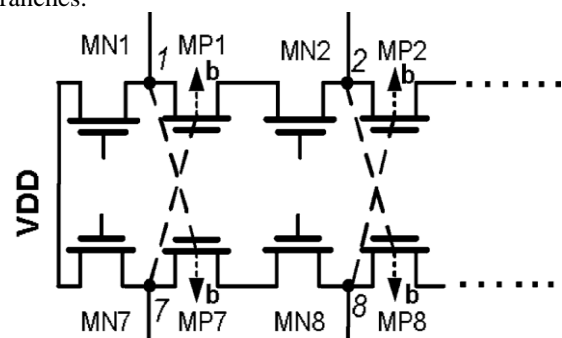

Fig.3. Body biasing from the node of operation

The clock supply and the input voltage (in milli volts) given to the first coupling of the inverter stage and then the body biasing node could be activated from the MN1 to MP7 and following to the all stages from the n-MOS to p-MOS. The second stage i.e the backward control and the reverse coupling of the MN2 from MN8 and also the MP2 from MP8. Then this node of operation can be better and improves when compared to the first node of operation. Then for the each level of stages can be amplified as per the backward control and the biasing node through the channel operation from the each number of stages.

This could be coupling and does not carry any dead zone of operation and this could be switching to the prominent to the all stages. The capacitance from the c1 of each branch carries the unit supply of the voltage from clk to clkb. Then the last stage from the n-MOS N1 and this could be coupling with the N2 and then the P1 coupling with the P2 having the amplitude switching. Then this storage from the each stages of the coupling from the node of operation can also to be calculated from the structural of the node 1 to 8. Then another node of bulk connection has been applied from the N1 to the P1 of linear stages. This could be effectively reduces the parasitic capacitance from the charge pump.

This charge pump has advantages of the low power consumption based on body biasing bulk connection from the each node of operation. And also this charge pump circuit has been enabled for the lower input voltage (in milli volts) having the bulk output voltages from the clock pulses. The enabling signals that carry the circuit level of operation from the amplitude degradation of the unit supply to the needed positive up gradation from the input amplitude. This phase difference from the clock pulses into the bulk connection from the unit supply that can be varied as per the input signal.

The required connection between these signals has been proposed and implemented into the phase locked loop. This could be having the phase detector, Charge pump and the voltage controlled oscillator. The level of connection is to be a feedback signal from the VCO to the input voltage. The phase difference from the input and the feedback signals has been applied to the phase detector. Then the charge pump gives the amplification of the input voltage from the phase detector. The variations of the phase frequency has been identified and also applied for the frequency synthesizer.

IV. MODIFICATIONS

A. SIX STAGE CHARGE PUMP WITH PLL IMPLEMENTATION

A phase-locked loop may be a feedback system combining a voltage controlled generator (VCO) and a phase comparator therefore connected that the generator maintains a relentless phase relative to a reference signal. Phase-locked loops are used, as an example, to come up with stable output high frequency signals from a set low-frequency signal.

A phase-locked loop (PLL) circuit is a motivating electronic building block wide employed in several integrated applications. It's typically employed in systems involving automatic management of frequency or part, like communications, frequency synthesis, radar, telemetry, and instrumentation systems. The PLL circuit generates associate output that tracks associate input reference signal. The output is synchronic with the input reference signal in frequency yet as in part.
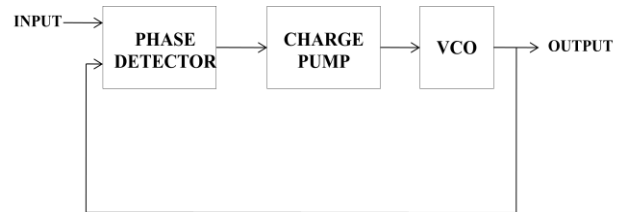

Fig.4. Block diagram of PLL with charge pump

Typically, a PLL is made around a part detector or part frequency detector (PFD), a charge pump, and a voltage-controlled generator (VCO) or current-controlled generator. The PLL can also embrace frequency dividers and mixers once employed in synthesizing frequency applications. The low-pass filter is needed to make sure the soundness and to see the information measure of the PLL by filtering the PFD output.

B. BANG-BANG PHASE DETECTOR WITH DCO

Bang-bang section detector primarily based section secured loops (PLL's) are getting additional and additional necessary in today's multi-gigabit communications systems. Additionally as having a simpler structure than their linear counterparts, bang-bang phase detectors will run at the very best speed AN IC fabrication process will build a operating flip flop. Moreover, since data is typically sampled as a section of their operation, they exhibit no systematic section error.
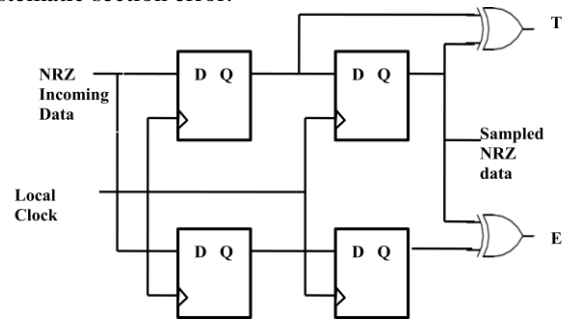

Fig.5. Bang-Bang phase detector

The Digital controlled generator (DCO) is that the core component of all digital part secured loop (ADPLL) system. Here, we have a tendency to propose DCO structures with digital management, reduced hardware and low power consumption. Totally different DCOs square measure supported ring based mostly topology having three, four & five management bits. Ranges of management bits will be accumulated as per the need of output frequency vary.

In DCO structures the periodic frequency is decided by digital input vector applied to DCDE. Controls

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switch network of NMOS/PMOS semiconductor units area unit placed at the sources/drain of NMOS/PMOS transistor of electrical converter delay cell.
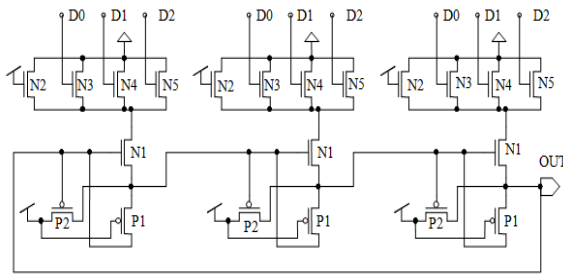

Fig.6. Three Bit DCO with Switching Networks

Relying upon the condition of input vector, the equivalent resistance of switch networks changes the delay of specific stage changes that more modulates the output frequency.

C. ALEXANDAR PHASE DETECTOR WITH LC TANK OSCILLATOR

The Alexander configuration is another example of PDs providing inherent knowledge retiming. Following our reasoning for the Hogged palladium, we note that this property needs that the info be sampled by the clock; however one DFF doesn't live up to. Nonetheless, if the clock strobes the info waveform at multiple points within the neck of the woods of expected transitions, the ensuing samples will provide the required information.
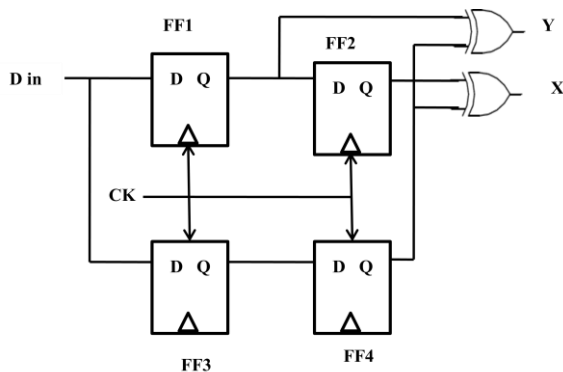

Fig.7. Alexander phase detector block

The many various styles of wave oscillators employed in radio and communication equipment, sometimes mistreatment some variety of resonant circuit to get signals at frequencies. Sine wave oscillators use LC elements because the frequency decisive device. A resonant LC circuit stores energy alternately within the electrical device and also the capacitor; this produces AN output that's curved.
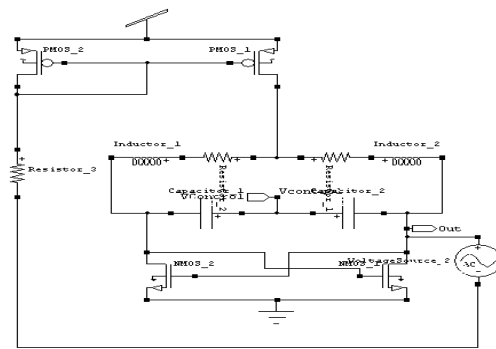

Fig.8. LC tank oscillator circuit

D. HOGGE PHASE DETECTOR WITH RING OSCILLATOR

The HOGGE topology may be a linear part detector, generating a small average as the part difference approaches zero. Thus, a charge pump driven by a Hogge PD experiences very little "activity" once the CDR loop is locked. This could be further used for the related applications into the details from the all the PLL's.
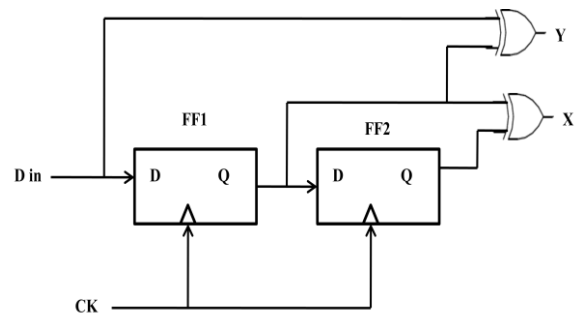

Fig.9. Block of HOGGE phase detector

Ring oscillators are the cascaded combination of delay stages connected in the close loop chain. This loop chains having the delay stages used for the numerous advanced features. This could be having the less power dissipation with less delay. Then also the integrated technology could be used as an easily. And also this can provide the multi-stage output for various structures.
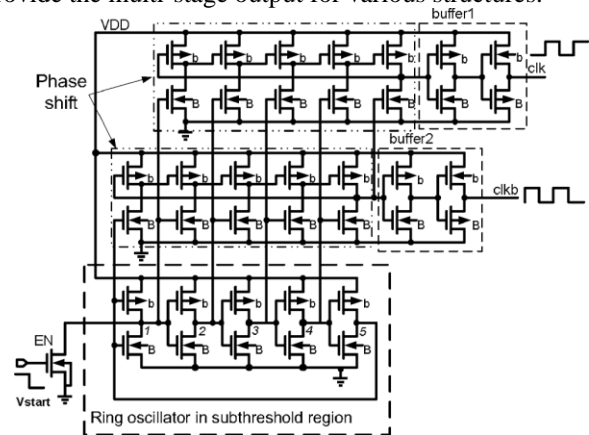

Fig.10. Ring oscillator circuit

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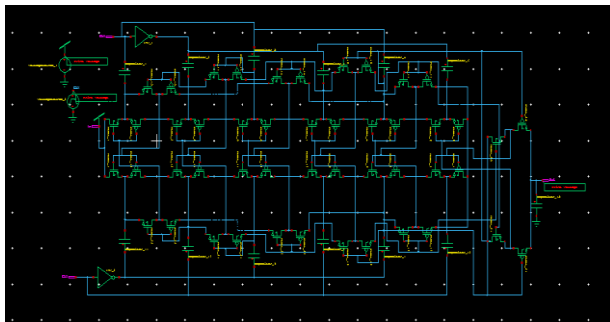
V.   SIMULATION RESULTS
VI.

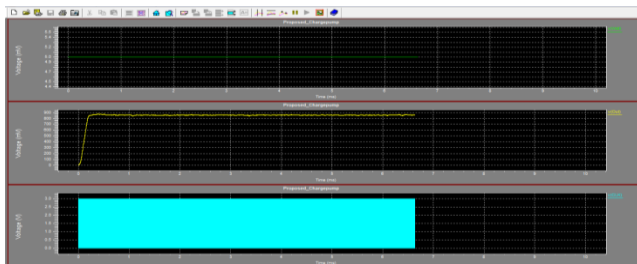*Fig.11.   Schematic of six stage charge pump*

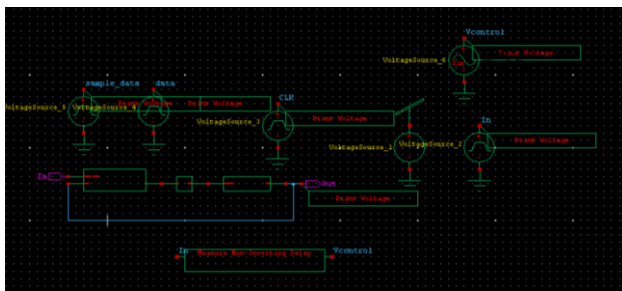*Fig.12.   Waveform of the six stage charge pump*

Fig.13. Schematic of six stage charge pump based PLL
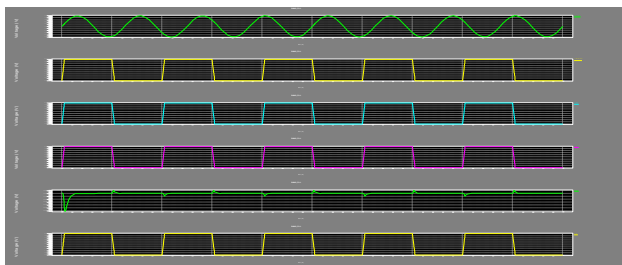

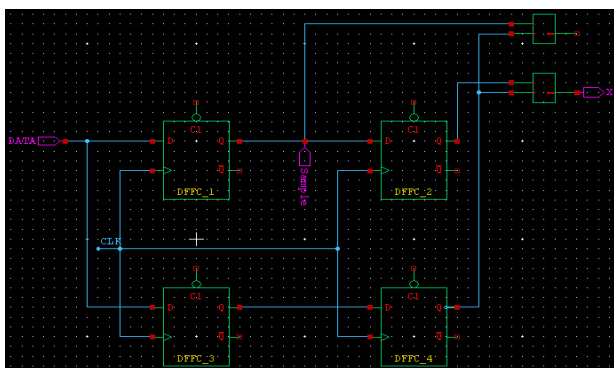*Fig.14. Waveform Of six stage charge pump based PLL*

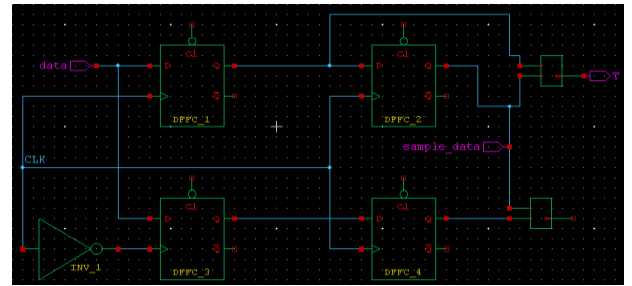*Fig.15. Implementation of Alexander phase detector*

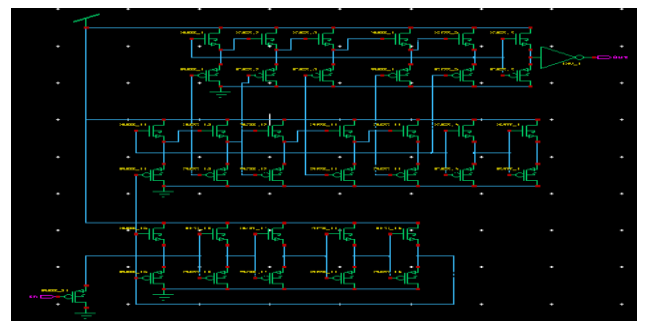*Fig.16. Implementation of Bang Bang phase detector*
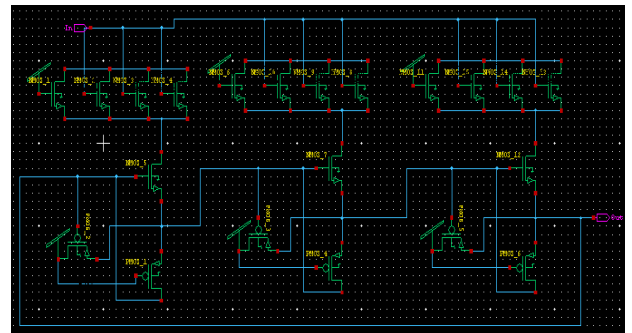

Fig.17. Implementation of Ring Oscillator

Fig.18. Implementation of DCO

TABLE-I
PARAMETER RESULTS OF THE SIX STAGE CHARGE PUMP PLL

TYPE OF PLL	DELAY (η s)	OUTPUT POWER (μ w)
Alexander- Ring	0.0425	0.049
Alexander- DCO	0.0425	0.071
Alexander- LC	0.0425	0.061
Bang Bang- Ring	0.0412	0.039
Bang Bang- DCO	0.0412	0.095
Bang Bang- LC	0.0412	0.034
Hogge- Ring	0.0525	0.041
Hogge- DCO	0.0525	0.024
Hogge- LC	0.0525	0.037

The results has been analyzed and verified for the six stage charge pump based PLL by applying each combination of phase detectors and oscillators. The capacitance of these charge pumps has been 1 pF. The technology of the NANO meter used here is TSMC018 CMOS. The input operating voltage is in the range of mV. The variation of the output amplitude voltage could be obtained from this charge pump of the clock signal to be applied to the input source.

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VII.   CONCLUSION

Charge pump based on body biasing and the backward control scheme has been proposed in this system. The power and the amplification could be efficient when compared to the other existing charge pump circuits. The low output ripple and high system stability of the dual-phase charge pump circuit are demonstrated by the test chip and get better performance. Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the charge pump circuit so as to improve the power conversion efficiency. The degradation of the amplification could be highly reduces and it could be generated as per the test identification stages proposed in the charge pump design circuit. The implementation could be used in the phase locked loops for the grid level applications. The block could be changed and the phase detectors are modified for the further reduction of power and the delay operations. The simulation result shows that the performance of six stage charge pump based PLL is better if it is implemented using Bang Bang phase detector and digitally controlled oscillator (DCO).

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