Abstract - This paper presents a novel fifteen level asymmetric MLI with lesser number of components. This inverter topology is asymmetric in nature and contains three unequal DC voltage sources. It consists of reduced semiconductor devices which reduce circuit complexity, installation area and cost of the system. The proposed topology also decreases Total Harmonic Distortion (THD) which leads to better efficiency and voltage stress on the devices will be decreased. The analysis is done with Half-height Pulse Width Modulation technique. The inverter is simulated in Matlab/Simulink Software.

Keywords - Asymmetric MLI; Pulse Width Modulation; Efficiency; Total Harmonic Distortion (THD).

I. INTRODUCTION

Multilevel inverters (MLI) are the most important tool of power converters used elaborately in high and medium power applications [1]. Compared to two level and three level inverters, multilevel inverters give the output voltage nearer to sinusoidal waveform. For this reason, the researchers have been proposing MLI topologies of higher levels. If frequency of switches is low, switching devices of multilevel inverters gives better performance and switching losses will be reduced [2-5].

Three classical topologies of multilevel inverters are Diode-clamped or Neutral- point- clamped (NPC) [6], Flying-capacitor (FC) [7] and Cascaded H-Bridge (CHB) [11]. But diode-clamped and flying-capacitor inverters suffer from dc-link voltage balancing problem, bulk size of capacitor and more number of semiconductor components in more levels.

The cascaded multilevel inverters provide an important solution to overcome limitations in operating voltage of the inverters. In this way, this kind of multilevel inverters current of switching devices is same as the output current. CHB multilevel inverter consists of many H-bridges which are connected in series, if the number of voltage levels increases number of semiconductor components also increases [8-10]. To overcome these problems, a novel 15-level MLI is presented on the basis of series connection of DC voltage sources. It consists of minimum number of IGBT switches and DC voltage sources. THD is also reduced. For 15-level output waveform proposed topology gives lower THD compared to other topologies [11-15].

II. PROPOSED MULTILEVEL INVERTER

The configuration for proposed MLI topology is shown in Fig. 1. It involves ten IGBT switches and three dc voltage sources to produce 15-levels in the output. This inverter topology uses three dc voltage sources $V_1$, $V_2$ and $V_3$ of values $V_{dc} \times 2V_{dc}$ and $4V_{dc}$. The switches $S_{c11}, S_{c12}, S_{c13}, S_{c21}, S_{c22}$ and $S_{c23}$ turns ON and OFF to generate 15 levels in the output of inverter. This section is known as level generation. It is possible to connect n number of IGBT switches in level generation section to produce n levels in the output voltage.

In order to change the polarity of the output waveform, a set of switches $S_1, S_4$ form H-bridge operates for positive half cycle and other set of switches $S_2, S_3$ operates for a negative half cycle. This section is called polarity generation. In this topology, maximum switches conducting at a time are four. Hence voltage stress on the semiconductor devices will be low.

![Fig. 1. Proposed MLI topology](image-url)

The operating principle for the proposed multilevel inverter is illustrated in Fig. 2. Current paths in the positive half cycle are represented by dark lines. The zero state in the circuit is obtained by turning ON the upper switches ($S_1$ and $S_3$) or lower switches ($S_2$ and $S_4$) of the H-bridge.
Fig. 2. Different modes of operation for output levels and current paths in the positive half cycle

During the positive half cycle, switches $S_1$ and $S_4$ are always ON, and switches $S_2$ and $S_3$ are OFF. Therefore, output voltage is positive. During the negative half cycle, switches $S_2$ and $S_3$ are always ON, and switches $S_1$ and $S_4$ are OFF. Hence, the output voltage is negative. Here, switches $S_1, S_2, S_3$...
and $S_4$ determine whether the output voltage is positive or negative. The details about the switching states and voltage levels of output for the proposed MLI topology are presented in Table I.

<table>
<thead>
<tr>
<th>Voltage levels</th>
<th>$S_{c11}$</th>
<th>$S_{c12}$</th>
<th>$S_{c21}$</th>
<th>$S_{c22}$</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>7$V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6$V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5$V_{dc}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4$V_{dc}$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3$V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2$V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$-V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$-2V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$-3V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$-4V_{dc}$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$-5V_{dc}$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$-6V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

From 270 degree to 360 degree, switching angles are calculated by the equation:

$$a_{2m-1} = \frac{2\pi - a_{m-1}}{2}, \frac{2\pi - a_{m-2}}{2}, \ldots, \frac{2\pi - a_1}{2}$$

For a 15-level inverter, the switching angles calculated for Half-Height PWM are: $a_1 = 4.096^\circ$, $a_2 = 12.37^\circ$, $a_3 = 20.92^\circ$, $a_4 = 30^\circ$, $a_5 = 40^\circ$, $a_6 = 51.78^\circ$ and $a_7 = 68.21^\circ$.

The switching angles for second (90 to 180 degree), third (180 to 270 degree) and fourth (270 to 360 degree) quadrant can be calculated by using above equations.

### III. PWM TECHNIQUE

Semiconductor devices in the MLI must be operated in such a way that appropriate output voltage levels are produced with reduced THD. Pulse width modulation techniques which are used in MLI are categorized based on frequency of switches. In this paper, Half-Height PWM method is used.

The Half-height (HH) PWM method can be explained as, when the fundamental value increases to the half-height of the level, the switching angle is set. In this method, the main switching angles are obtained by using the equation

$$a_i = \sin^{-1}\left(\frac{2i - 1}{m - 1}\right)$$

Where $i = 1, 2, 3, 4, \ldots, \frac{m-1}{2}$ and $m = \text{number of output voltage level}$. Switching angles calculated from 0 degree to 90 degree refers to main switching angles. Switching angles for second, third and fourth quadrants can be calculated as follows.

From 90 degree to 180 degree of the output waveform, the switching angles can be calculated by using the equation

$$a_{m+1} = \pi - a_{m-1}, \pi - a_{m-2}, \ldots, \pi - a_1$$

From 180 degree to 270 degree, switching angles are calculated as

$$a_m = \pi + a_1, \pi + a_2, \ldots, \pi + a_{m-1}$$

### IV. SIMULATION RESULTS

The analysis for proposed fifteen level asymmetric MLI is performed by Matlab/Simulink Software. The proposed inverter has 3 dc voltage sources and the set values are $V_1 = 10V$, $V_2 = 20V$ and $V_3 = 40V$. The fundamental output voltage frequency is 50Hz. The load resistance of 100Ω and inductance of 1mH is taken.

In this paper, Half-Height pulse width modulation technique is used to control the proposed multilevel inverter. Fig.3 shows the simulation model for proposed 15-level MLI. Fig. 4, represents 15 levels in the output of proposed inverter topology and Fig. 5, represents the FFT analysis of the output waveform by using Half-Height Pulse Width Modulation (PWM) method.

![Simulating Model for proposed 15-level MLI](image-url)
V. CONCLUSION

This paper presents a novel fifteen level asymmetric MLI. This proposed topology containing 10 IGBT switches and 3 dc voltage sources to produce 15 levels in the output of the inverter. It was shown that the proposed inverter uses reduced number of semiconductor elements as compared with other topologies, it also gives reduced THD and better efficiency. THD of the inverter is 5.48%, obtained by fundamental Pulse Width Method (PWM) like Half-Height method.

REFERENCES


Table II: Comparative study for different 15-level MLI topologies.

<table>
<thead>
<tr>
<th>Topologies</th>
<th>No. of levels</th>
<th>No. of switches</th>
<th>No. of DC sources</th>
<th>THD%</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>15</td>
<td>12</td>
<td>3</td>
<td>12.36</td>
</tr>
<tr>
<td>[13]</td>
<td>15</td>
<td>10</td>
<td>3</td>
<td>10.56</td>
</tr>
<tr>
<td>[14]</td>
<td>15</td>
<td>10</td>
<td>3</td>
<td>8.98</td>
</tr>
<tr>
<td>[15]</td>
<td>15</td>
<td>10</td>
<td>3</td>
<td>8.77</td>
</tr>
<tr>
<td>[16]</td>
<td>15</td>
<td>12</td>
<td>3</td>
<td>7.85</td>
</tr>
<tr>
<td>Proposed</td>
<td>15</td>
<td>10</td>
<td>3</td>
<td>5.48</td>
</tr>
</tbody>
</table>

From Table II, it can be concluded that the proposed topology showing better performance with respect to switching devices and Total Harmonic Distortion (THD) compared to other given topologies. In MLI topologies, as number of levels increases THD will reduces and reduced THD gives better efficiency and power quality.


