A Novel Fifteen Level Asymmetric MLI with Reduced Switching Devices and THD

Dr. Ramesh H R, Professor
Department of Electrical Engineering
University Visvesvaraya College of Engineering
Bengaluru, India

Bandhavya C S, P.G.Student
Department of Electrical Engineering
University Visvesvaraya College of Engineering
Bengaluru, India

***Abstract* - This paper presents a novel fifteen level asymmetric MLI with lesser number of components. This inverter topology is asymmetric in nature and contains three unequal DC voltage sources. It consists of reduced semiconductor devices which reduce circuit complexity, installation area and cost of the system. The proposed topology also decreases Total Harmonic Distortion (THD) which leads to better efficiency and voltage stress on the devices will be decreased. The analysis is done with Half-height Pulse Width Modulation technique. The inverter is simulated in Matlab/Simulink Software.**

Keywords* - *Asymmetric MLI; Pulse Width Modulation; Efficiency; Total Harmonic Distortion(THD).

I. INTRODUCTION

Multilevel inverters (MLI) are the most important tool of power converters used elaborately in high and medium power applications [1]. Compared to two level and three level inverters, multilevel inverters gives the output voltage nearer to sinusoidal waveform. For this reason, the researchers have been proposing MLI topologies of higher levels. If frequency of switches is low, switching devices of multilevel inverters gives better performance and switching losses will be reduced [2-5].

Three classical topologies of multilevel inverters are Diode-clamped or Neutral- point- clamped (NPC) [6], Flying-capacitor (FC) [7] and Cascaded H-Bridge (CHB) [11]. But diode- clamped and flying- capacitor inverters suffer from dc-link voltage balancing problem, bulk size of capacitor and more number of semiconductor components in more levels.

The cascaded multilevel inverters provide an important solution to overcome limitations in operating voltage of the inverters. In this way, these kind of multilevel inverters current of switching devices is same as the output current. CHB multilevel inverter consists of many H-bridges which are connected in series, if the number of voltage levels increases number of semiconductor components also increases [8-10]. To overcome these problems, a novel 15-level MLI is presented on the basis of series connection of DC voltage sources. It consists of minimum number of IGBT switches and DC voltage sources. THD is also reduced. For 15-level output waveform proposed topology gives lower THD compared to other topologies [11-15].

II. PROPOSED MULTILEVEL INVERTER

The configuration for proposed MLI topology is shown in Fig. 1. It involves ten IGBT switches and three dc voltage sources to produce 15-levels in the output. This inverter topology uses three dc voltage sources V_1, V_2 and V_3 of values $V_{dc}, 2V_{dc}$ and $4V_{dc}$. The switches $S_{c11}, S_{c12}, S_{c13}, S_{c21}, S_{c22}$ and S_{c23} turns ON and OFF to generate 15 levels in the output of inverter. This section is known as level generation. It is possible to connect n number of IGBT switches in level generation section to produce n levels in the output voltage.

In order to change the polarity of the output waveform, a set of switches S_1, S_4 form H-bridge operates for positive half cycle and other set of switches S_2, S_3 operates for a negative half cycle. This section is called polarity generation. In this topology, maximum switches conducting at a time are four. Hence voltage stress on the semiconductor devices will be low.

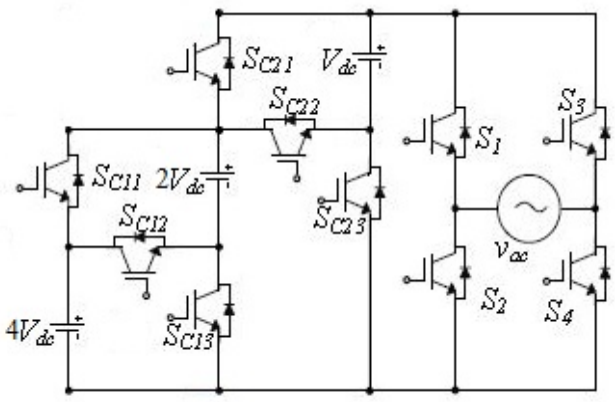
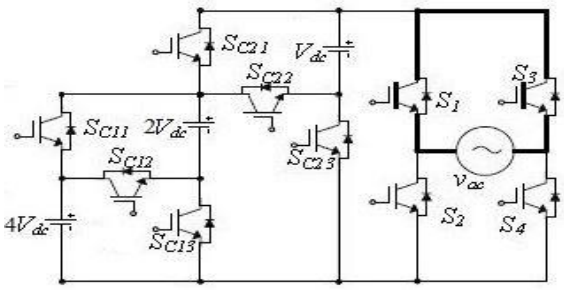
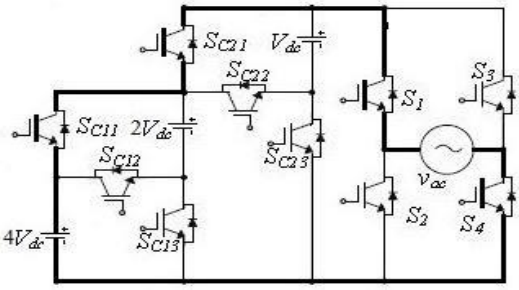


Fig. 1. Proposed MLI topology

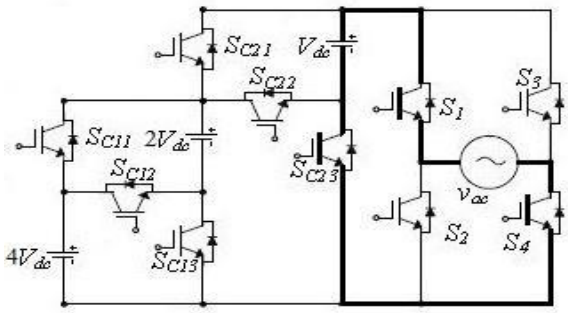
The operating principle for the proposed multilevel inverter is illustrated in Fig. 2. Current paths in the positive half cycle are represented by dark lines. The zero state in the circuit is obtained by turning ON the upper switches (S_1 *and* S_3) or lower switches (S_2 *and* S_4) of the H-bridge.



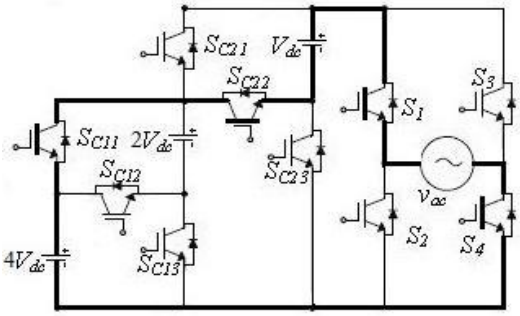
(Mode 1- 0V)



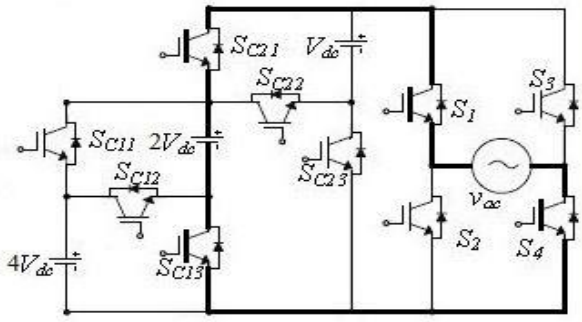
(Mode 5- $4V_d$)



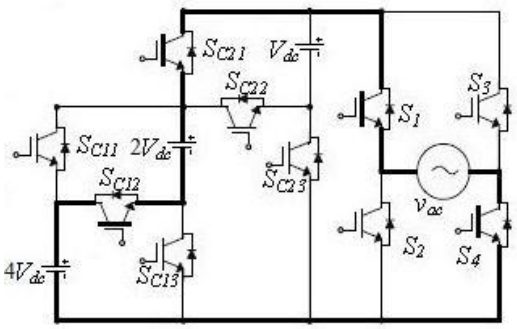
(Mode 2- V_d)



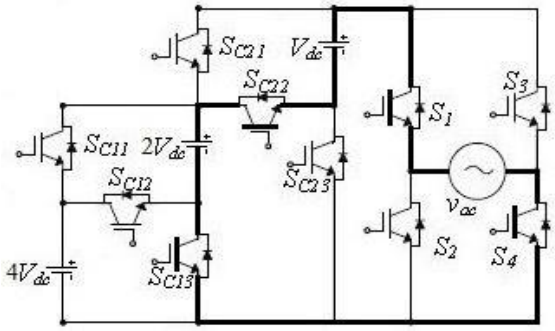
(Mode 6- $5V_d$)



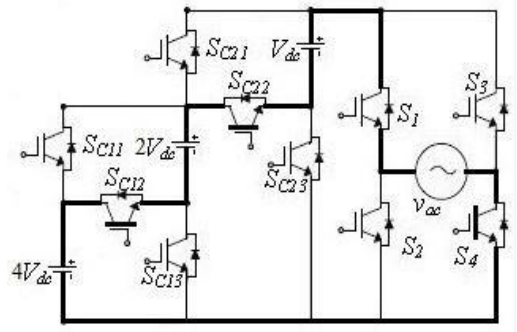
(Mode 3- $2V_d$)



(Mode 7- $6V_d$)



(Mode 4- $3V_d$)



(Mode 8- $7V_d$)

Fig. 2. Different modes of operation for output levels and current paths in the positive half cycle

During the positive half cycle, switches S_1 and S_4 are always ON, and switches S_2 and S_3 are OFF. Therefore, output voltage is positive. During the negative half cycle, switches S_2 and S_3 are always ON, and switches S_1 and S_4 are OFF. Hence, the output voltage is negative. Here, switches S_1, S_2, S_3

and S_4 determine whether the output voltage is positive or negative. The details about the switching states and voltage levels of output for the proposed MLI topology are presented in Table I.

TABLE I

SWITCHING STATES AND CORRESPONDING OUTPUT VOLTAGE LEVELS

Voltage levels	Switching states (ON=1, OFF=0)									
	S_{c11}	S_{c12}	S_{c13}	S_{c21}	S_{c22}	S_{c23}	S_1	S_2	S_3	S_4
$7V_d$	0	1	0	0	1	0	1	0	0	1
$6V_d$	0	1	0	1	0	0	1	0	0	1
$5V_d$	1	0	0	0	1	0	1	0	0	1
$4V_d$	1	0	0	1	0	0	1	0	0	1
$3V_d$	0	0	1	0	1	0	1	0	0	1
$2V_d$	0	0	1	1	0	0	1	0	0	1
V_d	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	0	0	1	0	1	0
	0	0	0	0	0	0	0	1	0	1
$-V_d$	0	0	0	0	0	1	0	1	1	0
$-2V_d$	0	0	1	1	0	0	0	1	1	0
$-3V_d$	0	0	1	0	1	0	0	1	1	0
$-4V_d$	1	0	0	1	0	0	0	1	1	0
$-5V_d$	1	0	0	0	1	0	0	1	1	0
$-6V_d$	0	1	0	1	0	0	0	1	1	0
$-7V_d$	0	1	0	0	1	0	0	1	1	0

III. PWM TECHNIQUE

Semiconductor devices in the MLI must be operated in such a way that appropriate output voltage levels are produced with reduced THD. Pulse width modulation techniques which are used in MLI are categorized based on frequency of switches. In this paper, Half-Height PWM method is used.

The Half-height (HH) PWM method can be explained as, when the fundamental value increases to the half-height of the level, the switching angle is set. In this method, the main switching angles are obtained by using the equation

$$a_i = \sin^{-1}\frac{(2i-1)}{(m-1)}$$

Where i=1, 2, 3, 4……$\frac{m-1}{2}$ and m= number of output voltage level. Switching angles calculated from 0 degree to 90 degree refers to main switching angles. Switching angles for second, third and fourth quadrants can be calculated as follows.

From 90 degree to 180 degree of the output waveform, the switching angles can be calculated by using the equation

$$a_{\frac{m+1}{2}} = \pi - a_{\frac{m-1}{2}}, \pi - a_{\frac{m-2}{2}} \ldots\ldots\ldots, \pi - a_1$$

From 180 degree to 270 degree, switching angles are calculated as

$$a_m = \pi + a_1 \ldots\ldots, \pi + a_{\frac{m-1}{2}}$$

From 270 degree to 360 degree, switching angles are calculated by the equation

$$a_{\frac{3m-1}{2}} = 2\pi - a_{\frac{m-1}{2}}, 2\pi - a_{\frac{m-2}{2}} \ldots\ldots, 2\pi - a_1$$

For a 15-level inverter, the switching angles calculated for Half-Height PWM are: $a_1 = 4.096^\circ$, $a_2 = 12.37^\circ$,$a_3 = 20.92^\circ$,$a_4 = 30^\circ$, $a_5 = 40^\circ$, $a_6 = 51.78^\circ$ and $a_7 = 68.21^\circ$.

The switching angles for second (90 to 180 degree), third (180 to 270 degree) and fourth (270 to 360 degree) quadrant can be calculated by using above equations.

IV. SIMULATION RESULTS

The analysis for proposed fifteen level asymmetric MLI is performed by Matlab/Simulink Software. The proposed inverter has 3 dc voltage sources and the set values are $V_1 = 10V$, $V_2 = 20V$ and $V_3 = 40V$. The fundamental output voltage frequency is 50Hz. The load resistance of 100Ω and inductance of 1mH is taken.

In this paper, Half-Height pulse width modulation technique is used to control the proposed multilevel inverter. Fig.3. shows the simulation model for proposed 15-level MLI. Fig. 4, represents 15 levels in the output of proposed inverter topology and Fig. 5, represents the FFT analysis of the output waveform by using Half-Height Pulse Width Modulation (PWM) method.

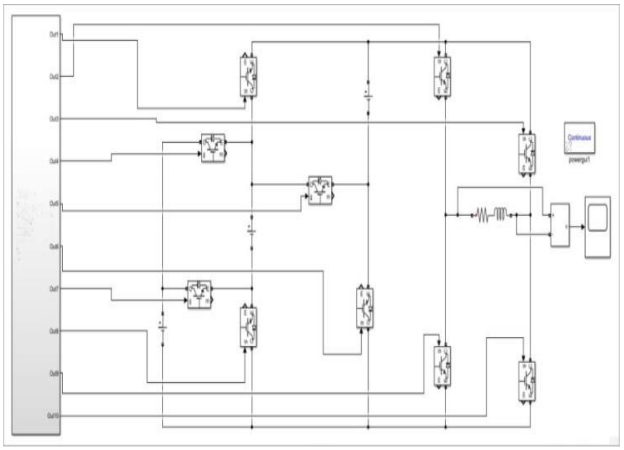


Fig. 3. Simulation Model for proposed 15-level MLI

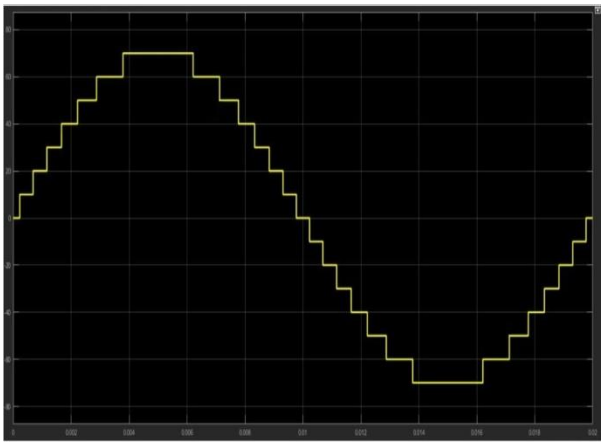


Fig. 4. Output waveform for proposed MLI

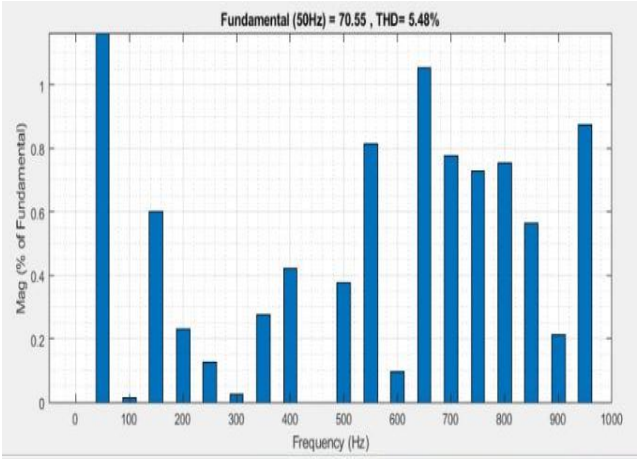


Fig. 5. Harmonic analysis of output waveform

Comparison of THD for different topologies

Table II: Comparative study for different 15-level MLI topologies.

Topologies	No. of levels	No. of switches	No. of DC sources	THD%
[12]	15	12	3	12.36
[13]	15	10	3	10.56
[14]	15	10	3	8.98
[15]	15	10	3	8.77
[16]	15	12	3	7.85
Proposed	15	10	3	5.48

From Table II, it can be concluded that the proposed topology showing better performance with respect to switching devices and Total Harmonic Distortion (THD) compared to other given topologies. In MLI topologies, as number of levels increases THD will reduces and reduced THD gives better efficiency and power quality.

V. CONCLUSION

This paper presents a novel fifteen level asymmetric MLI. This proposed topology containing 10 IGBT switches and 3 dc voltage sources to produce 15 levels in the output of the inverter. It was shown that the proposed inverter uses reduced number of semiconductor elements as compared with other topologies, it also gives reduced THD and better efficiency. THD of the inverter is 5.48%, obtained by fundamental Pulse Width Method (PWM) like Half-Height method.

REFERENCES

[1] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A Review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135-151, 2016.

[2] Song. W, Huang. A. Q, "Fault-tolerant designed control strategy for cascaded H-bridge multilevel converter-based STATCOM," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, 2010, pp. 2700-2708.

[3] Selvaraj. J, and N. A. Rahim, "A Novel Pulse Width Modulation (PWM) for Grid-connected Multilevel Inverter," *Journal of Renewable and Sustainable Energy*, no. 5, pp. 053102, 2009.

[4] Arani, A. A. Khodadoost, H. R. Zaferani, M. J. Sanjari, and G. B. Gharehpetian, "Using genetic algorithm and simulated annealing for 27-level PV inverter THD minimization," *Smart Grid Conference (SGC)*, pp. 1-6, 2014.

[5] Sirisukprasert. S, Jih-sheng Lai, Tian-Hua Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 875-881, 2002.

[6] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral point clamped inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2219-2230, 2010.

[7] H. Jing, and K. A. Corzine, "Extended operation of flying-capacitor multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 21, pp. 140-147, 2006.

[8] P. W. Hammod, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Transactions on Industrial Applications*, vol. 33, no. 1, pp. 202-208, Jan/Feb. 1997.

[9] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel inverters," in *Conference Rec. IEEE Ind. Appl. Soc. Annu. Meeting*, 1999, vol. 2, pp. 1186-1192.

[10] R. H. Osman, "A medium voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meeting*, 1990, pp. 2662-2669.

[11] D. R. Trainer, "Static Var Compensator (STATCOM) based on single phase chain circuit converters," *Proc. Inst. Elect. Eng.-Generation Transmission Distribution*, vol. 145, no. 4, pp. 381-386, July 1998.

[12] Mohammad Eydi, Mohammad-Ali Salahmanesh, Seyyed Hossein Hosseini, and Reza Ghazi, "A novel structure for 15-level inverter based on CHB and SCMLI topology," in *11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*, IEEE, 2020.

[13] Smitha Singhai, Avinash Pandey, Varsha Singh, "New topology of asymmetrical multilevel inverter [15/29 level]," in *International conference on Current Trends Converging Technologies (ICCTCT)*, IEEE, 2018.

[14] Malik Qamar Abbas, Abdul Majib, Jawad Saleem, and Muhammad Arif, "Design and analysis of 15-level asymmetric multilevel inverter with reduced switch count using different PWM techniques," in *International Conference on Frontiers of Information Technology (FIT)*, IEEE, 2017.

[15] V. Premsai Reddy, K. Muralikumar, P. Ponnambalam, and Ashutos Mahapatra, "Asymmetrical 15-level multilevel inverter with fuzzy controller using super imposed carrier PWM," in *Conference on Innovation in Power and Advanced Computing Technologies (i-PACT)*, IEEE, 2017.

[16] Kuldeep Rathore, and Praveen Bansal, "A new 15-level asymmetrical multilevel inverter topology with reduced number of devices for different PWM techniques," in 2nd *International Conference on Power*

Electronics, Intelligent Control and Energy Systems (ICPEICES), IEEE, pp. 355-360, 2018.

[17] Md N. H. Khan, M. Forouzesh, Y. P. Siwakoti, and F. Blaabjerg, "Switched-capacitor integrated (2n+1)-levels step-up single-phase inverter," *IEEE Transactions on Power Electronics*, vol. 33, pp. 2963-2972, 2019.

[18] R. Ramaprabha, S. Malathy, and Ramya Krishnan, "A 17-level asymmetric multilevel inverter with fundamental frequency PWM schemes," in *2nd International Conference on Power and Embedded Drive Control (ICPEDC),* IEEE , pp. 510-515, 2017.

[19] S. R. Raman, Y. Ye, and K. E. Cheng, "Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution," *IEEE Transactions on Power Electronics,* vol. 33, no. 7, pp. 5937-5948, July 2018.

[20] E. Babaei, M. F. Kangarlu, F. N. Mazgar, "Symmetric and asymmetric multilevel inverter topologies with reduced switching devices," *Elsevier Electr. Power Syst. Res*., vol. 86, pp. 122-130, 2012.

[21] J. Rodriguez, J. Lai, F. Z. Peng, "Multilevel inverter: a survey of topologies, controls and applications," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 724-738, 2002.

[22] Gupta, Krishna Kumar, et al, "Multilevel inverter topologies with reduced device count: A review," *IEEE Transactions on Power Electronics,* vol. 31, no. 1, 2016, pp. 135-151.

[23] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits and Systems Magazine,* vol. 1, pp. 37-42, 2001.

[24] P. Kala, and S. Arora, "A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications," *Renewable and Sustainable Energy Reviews,* vol. 76, pp. 905-931, 2017.

[25] H. Taghizadeh and M. TarafdarHagh, "Harmonic elimination of cascade multilevel inverters with non-equal DC sources using particle swarm optimization," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 11, pp. 3678-3684, 2010.