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A Novel FGMOS Voltage Reference with Temperature and Power Supply Compensation

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Abstract

In this paper, we propose a scheme for generating a reference voltage which can be implemented in the CMOS technology. The system performance is investigated for a range of supply voltages and temperature. The system performance is improved by the use of floating gate MOSFET. The work includes mathematical modeling of the proposed voltage reference circuit and its verification by simulation using TANNER EDA tools. The circuit performance over temperature and supply voltage is better than the prior works in this area. The reference voltage is obtained by combining the weighted V_{GS} difference with weak-inversion V_{GS} voltage, which has a negative temperature coefficient. This circuit provides a nominal reference voltage of 458mV, temperature coefficient of 10 ppm/^oC in [20^oC ~ 120^oC] at a 0.8 V supply voltage. The line regulation of the reference voltage is 5.6mV/V when the supply voltage is increased from 0.8 V to 2 V.

1. Introduction

IN many applications, a precise and stable reference voltage is widely used in digital and analog circuits like analog–digital (A/D) and digital–analog (D/A) converters, voltage regulators, DRAM/flash memories and other communication devices. The demands for smaller area, low power consumption and low sensitivity to the supply voltage and temperature are getting increased. Recently, the voltage reference circuits were proposed to achieve smaller area without resistors [7], or low power supply, such as 1 V [8], [9]. However, all of them require big-area diodes or parasitic bipolar junction transistors (BJTs) with turn-on voltage as high as 0.6 V at room temperature. Thus, some people started to exploit MOSFETs operated in subthreshold region to generate the reference voltage independent of the power supply and temperature. Parts of reference circuits can further be configured to serve as on-chip die temperature monitors, e.g. on large digital microprocessors. Recently, Filanovsky and Allam has studied the MOSFET temperature behavior by emphasizing the relationship between the I-V characteristic of a MOSFET biased in saturation region and temperature [1]. In this, they pointed out clearly that below a certain bias point, the gate-source voltage of a MOSFET, biased with a fixed drain current, decreases with temperature in a quasi-linear fashion. Starting from this observation, a gate-source voltage can be used instead of a base-emitter voltage to design a voltage reference independent of temperature. Many researchers have proposed several low-power and low-voltage reference circuit solutions based on weak-inversion MOSFETs [2],[3]. The effect of temperature in the weak inversion characteristics of MOSFET's is discussed [4]. In this paper, a low temperature coefficient FGMOS voltage reference circuit is presented. The reference circuit generates the voltage with positive temperature coefficient from weighted V_{GS} difference between two NMOSFETs in the weak inversion region while the voltage with negative temperature coefficient is obtained by the weak inversion V_{GS} voltage. With the MOSFETs operating in the weak inversion, the reference circuit consumes less current and thus reduces the power consumption.

The floating mosfet is presented in section 2, proposed voltage reference circuit is illustrated in section 3. Simulation results are presented and compared with previous work in Section 4. Section 5 concludes the paper.

2. Floating Gate MOSFET

A Floating Gate MOS Transistor consists of a conventional MOS transistor with its gate surrounded by SiO_2 and capacitively coupled to multiple controlling input gates [11]-[14].Since the gate surrounded by SiO_2 has no DC path to a fixed potential, it is known as Floating Gate. ie, The floating gate is formed by the first polysilicon layer, while the multiple-input gates are formed by the second polysilicon layer located above the floating gate. The conduction of the FGMOS transistor is different from that of conventional MOS transistor having the same terminal potential, due to the capacitive coupling between the Floating Gate and control gates. When a voltage is applied to the control gates, capacitive coupling between the control gate and Floating Gate induces an electrical field on the Floating Gate (FG). The induced field on the Floating Gate modifies the conductance of underlying channel region.

A two input Floating Gate MOSFET is shown in Fig.1 where a dc voltage (V_b) is applied at one of the gates called bias gate (BG) while the signal is applied at second gate termed as signal gate (SG).

The resultant threshold voltage $V_T(fg)$ of the FGMOS [8] with respect to signal gate, depends on the threshold voltage of the Floating Gate (V_T) and is given in (1).

$$V_T(fg) = \frac{V_T - V_T k_1}{k_1} \quad (1)$$

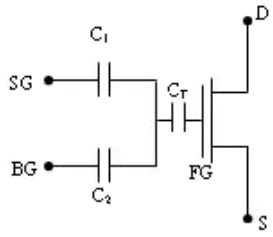

Fig.1. Two input Floating Gate MOSFET structure

Where $k_1 = c_1 = c_T$ $k_2 = c_2 = c_T$, C_1 and C_2 represent the capacitances between floating gate and control gates respectively, C_T is the sum of all the capacitances between control gates and floating gate, capacitance between floating gate to drain, capacitance between floating gate to source and capacitance between floating gate to bulk.

3. Proposed Voltage Reference

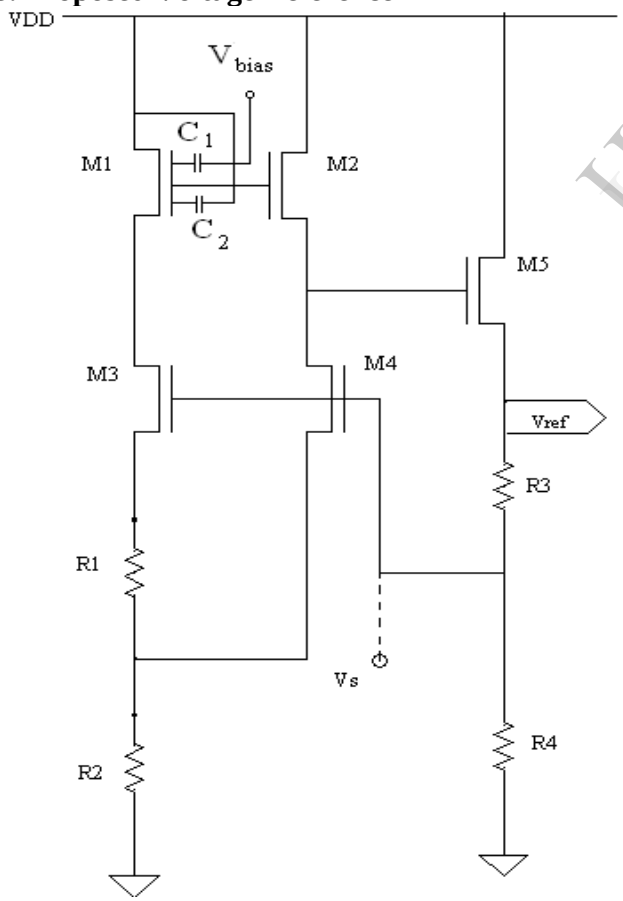

Fig. 2. Schematic of proposed voltage reference circuit.

The proposed voltage reference circuit is shown in Fig. 2. Transistors M_1 and M_2 are connected as a FGMOS current mirror and served for realizing the function of self-biasing. The current mirror of M_1 and M_2 is designed to make MOSFETs M_3 and M_4 operate in the weak inversion such that the voltage across R_1 is proportional to the absolute temperature (PTAT). Hence, the resistor ratio R_2/R_1 can be used to compensate for the variation of the gate-source voltage of M_4 with respect to the temperature.

For an n-MOSFET operating in the weak-inversion region, with the condition of $V_{DS} \geq 3V_T$, its drain current can be given as[5],[6]:

$$I_D = \frac{W}{L} I_t \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \quad (2)$$

where $I_t = qXD_n N_{qo} \exp(C/V_T)$, V_{th} is the threshold voltage, n is the subthreshold slope factor, X is the thickness of the region in which I_D flows, D_n is the diffusion constant for electrons, N_{q0} is the equilibrium concentration of electrons in the substrate, $V_T = kT/q$ is the thermal voltage, and C is a constant.

The drain current of M_3 and M_4 can be expressed as

$$I_{D3} = K_3 I_t \exp\left(\frac{V_{GS3} - V_{th}}{nV_T}\right) \quad (3)$$

$$I_{D4} = K_4 I_t \exp\left(\frac{V_{GS3} - V_{th}}{nV_T}\right) \quad (4)$$

where $K_i = (W/L)_i$ and $K_3 = NK_4$. Using (2) and (3) assuming that the ratio of K_1 and K_2 is unity which means that the current flowing into M_3 and M_4 are equal, we can obtain

$$V_{GS4} - V_{GS3} = nV_T \ln(N) \quad (5)$$

From Fig. 1, the two gate-source voltages of M_3 and M_4 are also related by

$$V_{GS4} = V_{GS3} + I_{D3} R_1 \quad (6)$$

Substituting (4) into (5), we obtain

$$I_{D3} = \frac{V_{GS4} - V_{GS3}}{R_1} = \frac{nV_T \ln(N)}{R_1} \quad (7)$$

(6) shows that the drain current of M_3 is proportional to the absolute temperature(PTAT). The gate voltage V_S of M_3 and M_4 is given as:

$$V_S = V_{GS4} + 2I_{D3} R_2 \quad (8)$$

For an n-MOSFET with PTAT drain current, we can obtain the expression of V_{GS} from (1):

$$V_{GS} = nV_T \ln\left(\frac{I_D}{\frac{W}{L}I_t}\right) + V_{th} \quad (9)$$

Substituting (8) into (5), we obtain

$$V_{GS4} = nV_T \ln\left(\frac{I_{D3}}{K_3 I_t}\right) + V_{th} + I_{D3}R_1 \quad (10)$$

With the source and bulk terminals connected together, we could have the expression of V_{th} as follows [6].

$$V_{th} = \frac{\sqrt{2qN_A\varepsilon(2\phi_f)}}{C_{ox}} + 2\phi_f + \phi_{ms} - \frac{Q_{ss}}{C_{ox}} \quad (11)$$

Because ϕ_{ms}, Q_{SS}, and C_{OX} are independent of temperature, differentiating (10) gives

$$\frac{dV_{th}}{dT} = -\frac{1}{T_0}\left[\frac{E_g}{2q} - \phi_f\right]\left[2 + \frac{\gamma}{\sqrt{2\phi_f}}\right] \quad (12)$$

where N_A is the doping density, ε is the permittivity, φ_f is the Fermi level, C_{OX} is the gate oxide capacitance, φ_{ms} is the work function difference existing between the gate metal and the silicon, Q_{SS} is the positive charge density existing in the oxide at the silicon interface, E_g is the band gap of silicon at T =0°K, and γ is defined as[6] $\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon N_A}$.

Equation (11) shows that the threshold voltage reduces with the increase of the temperature since $\varphi_f < E_g/2q$. Thus, we could say that the threshold voltage V_{th} has a negative temperature coefficient. Substituting (6) and (9) into (7), the voltage V_S can be expressed as

$$V_S = nV_T \ln\left(\frac{I_{D3}}{K_3 I_t}\right) + V_{th} + I_{D3}R_1 + 2I_{D3}R_2$$

$$= nV_T \ln\left(\frac{I_{D3}}{K_3 I_t}\right) + V_{th} + \left(\frac{nV_T \ln(N)}{R_1}\right)(R_1 + 2R_2)$$

$$= nV_T \ln\left(\frac{nV_T \ln(N)}{K_3 I_t R_1}\right) + V_{th} + \frac{nV_T \ln(N)}{R_1}\left(R_1 + 2\frac{R_2}{R_1}\right) \quad (13)$$

Hence, the size K_3 of M_3, the resistor ratio R_2/R_1, and the aspect ratio N of M_3 and M_4 can be designed to make the temperature coefficient of V_S equal to zero at a selected temperature. Therefore, the final output reference voltage V_{ref} can be expressed as

$$V_{ref} = \left(1 + \frac{R_3}{R_4}\right)V_S \quad (14)$$

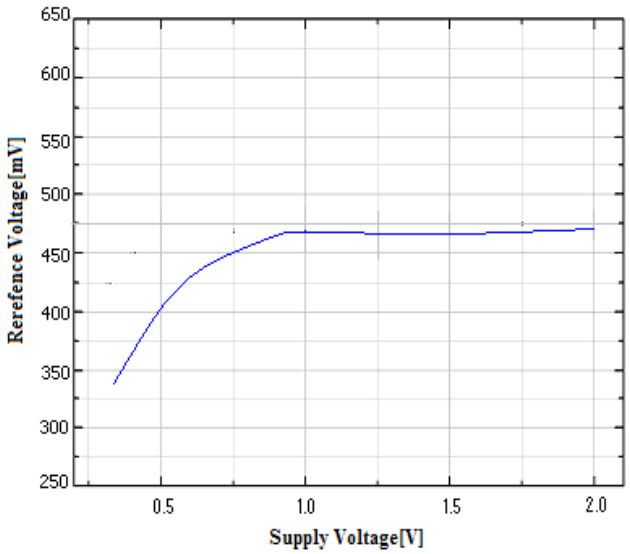

Fig. 3. Reference voltage against supply voltage

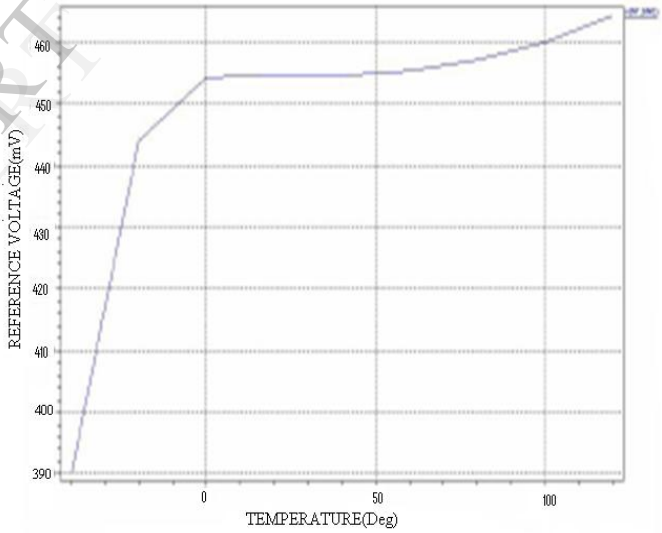

Fig. 4. Reference voltage against temperature at supply voltage.

TABLE 1.COMPARISON WITH PREVIOUS WORK

parameter	Proposed work	Previous Work[5]
Minimum supply voltage	0.8V	1.5V
Reference voltage	458mV	580mV
Temperature coefficient	10 ppm/°C	62 ppm/°C
Line regulation	5.6mV/V(0.8V~2V)	8mV/V(1.5V~3V)

4. Simulation Results

Fig. 3 shows the simulation result of the reference voltage V_{ref} against supply voltage at room temperature. The circuit is simulated using TANNER EDA tools with BSIM 4.4 model . The reference voltage is independent of supply voltage when the supply voltage Reaches near 0.8V. The line regulation is 5.6 mV/V when the supply voltage is increased from 0.8V to 2V.The temperature coefficients of the reference voltage V_{ref} against temperature is obtained 10ppm/°C at 0.8V supply voltage. Fig. 4 shows the simulation results of the reference voltage V_{ref} against temperature supply voltage. Table 1 shows comparison of proposed work with previous work [5] in terms of reference voltage, temperature coefficient and line regulation.

5. Conclusion

A low-power, low temperature coefficient FGMOS voltage reference circuit with MOSFETs operating in the subthreshold region is presented. The voltage reference is also independent of supply voltage 0.8V and temperature. Simulated reference output voltage is around 458mV and the minimum supply voltage is 0.8V. The temperature coefficient is 10ppm/°C from 20°C~120°C and the line regulation is 5.6mV/V from 0.8V to 2V. The circuit has been simulated using TANNER EDA tools with BSIM 4.4 model.

REFERENCES

[1] M. Filanovsky, A. Allam, "Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits," *IEEE Trans. on Circuits and Systems – I: Fundamental Theory and Applications, Vol. 48, No. 7, pp. 876-884, Jul. 2001.*

[2] G. Giustolisi, G. Palumbo, M. Criscione, and F.Cutrì,"A Low-Voltage Low-Power Voltage Reference Based on Subthreshold MOSFETs,"*IEEE Journal of Solid State Circuits, Vol. 38, no. 1,January 2003.*

[3] U. Yodprasit and J. Ngarmnil, "Efficient Low-Power Designs using MOSFETs in the weak inversion region", *IEEE Asia-Pacific Conference on Circuits, 1998*

[4] M. Nishida and H. Ohyabu, "Temperature Dependence of MOSFET Characteristics in Weak Inversion" , *IEEE Transactions On Electronic Devices, Vol. Ed 24,No.10,October1977.*

[5] M.H. Cheng, and Z.W. Wu, "Low-power low-voltage reference using peaking current mirror circuit," *ELECTRONICS LETTERS, Vol. 41, No.10, May 2008.*

[6] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, "Analysis and design of analog integrated circuits," *New York, John Wiley & Sons ,Inc., Fourth Edition, 2001.*

[7] Razavi, B.: 'Design of analog CMOS integrated circuits' (McGraw-Hill,New York, 1994).

[8] A. Buck, C. McDonald, S. Lewis, and T. R. Viswanathan, "A CMOS bandgap reference without resistors," in *Proc. IEEE Int. Solid-state Circuits Conf.*, 2000, pp. 442–443.

[9] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation,"*IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 670–674, Jun. 1999.

[10] A. Boni, "Op-Amps and startup circuits for CMOS bandgap references with near 1-V supply," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp.1339–1343, Oct. 2002.

[11] P. Hasler, T. S. Lande, "Overview of floating gate devices, circuits and systems", IEEE J. Solid State Circuits, vol. 48, no.1, pp. 1-3, Jan 2001.

[12] Paul Hasler. "Floating Gate Devices, Circuits, and Systems", IEEE Cmputer society , Proc. 9th International Database Engineering and Applications Symp. (IDEAS' 05), 2005.

[13] S. Tuan Wang, "On the I-V characteristics of floating gate MOS transistor", IEEE Trans. Elect. Devices, vol. 26, no. 9, pp. 1292-1294,Sept. 1979.

[14] Venkatesh Srinivasan, G. Serrano, C. M. Twigg, Paul Hasler, "A Floating gate Based Programmable CMOS reference", IEEE Trans.Circuits Syst.I, Reg. Papers, vol. 55, no. 11, pp. 3448-3456, Dec. 2008.