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A Novel Design of Modular Adder using NRA and RNA Reversible Logic gates for High speed Application

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***Abstract*-In digital world need for low power and high speed compatible device has been increased. This has turned the attention towards research in the field of reversible logic gates. This paper deals with the design of modular adder which would speed up the addition process. The use of reversible logic gate had made the design easier. Regularly the Fredkin gate and Feynman gates are used for permutation and copy operation. We propose a design based on the NRA and RNA. The combination of these two gates is called MCRG(memory compressive reversible logic gate) for implementing modular adder which performs a modular operation with reduced hardware complexity. The speed improvement is analyzed and compared with the existing designs using NRA&RNA reversible logic gate. In Proposed design, we have implemented MCRG to have reduced area, delay, speed, and garbage outputs.**

Keywords: NRA;RNA;,MCR;Modular adder

I. INTRODUCTION

The reversible logic gate is the one which has an equal number of inputs and outputs. A reversible logic gate totally differs from the normal universal gate. It has the ability to perform every operation as a normal gate and it is easy to implement and design. The two important rules for reversible logic gate: It should be able to produce the output from the input as well as reproduce the input from the output with zero power consumption. The input and output should be capable of being retained and operates in the reverse of the usual direction. Advantages of reversible logic gates are they reduce the power wastage. It connects with the other gates without loops and fanouts. The existing reversible logic gate are Toffoli, Fredkin, Feymann, Peres, NFT, BJN, NG, TSG, F2G, COG, HNG, modified Islam gate,MKG,ALG,DKG etc..,

Generally the adders can be divided into half and full adder depending on the number of inputs and the output(sum and carry) is same for both the adder. Different types of the adder in VLSI are Ripple carry adder, Carry save adder, Carry increment adder, Carry select adder, Carry skip adder, Carry look ahead adder, Carry bypass adder and so on. We can classify the modular adder into a general modular adder and special modular adder depending on the form of modules.

RNS stands for Residue number system which is used to perform the parallel computation of a system. In normal division, we take quotient as the output but in modulus operation, we take the remainder as the output. For modular RNS, first we should take a number'x' and then the co-prime number for the given number'x1,x2,x3' followed by the modulus operation(x/x1,x/x2,x/x3).we will get a module set that is the output of modular RNS operation which will be used for further calculations(addition).In a digital circuit, adders are used for performing a boolean operation using logic gates. In analog, it is used for adding analog voltages. Because of the use of an adder the operating speed is improved.

Among several adders carry look ahead adder is the fastest adder. Implementation and design of carry save, carry select and carry skip using proposed NRA, RNA - MCRG gates for modular addition based on RNS is implemented and designed.

II. EXISTING SYSTEM

A.Available reversible logic gate:
Depending on the application/requirement we can choose the type and number of gates.

Currently available reversible logic gates are 2×2,3×3,4×4,5×5. Some of them are listed below:

A. DKG

It is a 4*4 gate which has four input and four output.[2]

Fig 1. DKG

Inputs for the above gate is 0,A,B,C and Output is P,Q,R,S.

B.R-R gate
It is a 4*4 gate which has four input and four output.[4]

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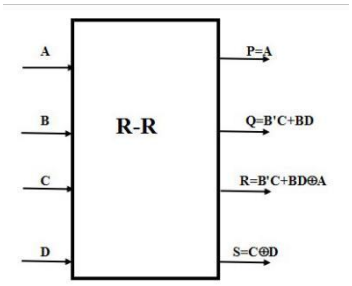

Fig 2. R-R

Inputs for the above gate is 0,A,B,C and Output is P,Q,R,S.Quantum cost is 6.

C. PAREEK

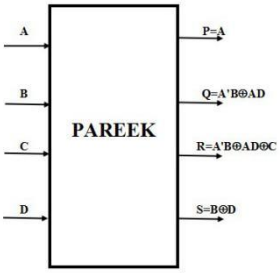

Fig 3. PAREEK

It is a 4*4 gate which has four input and four output.
Inputs for the above gate is 0,A,B,C and Output is P,Q,R,S.Quantum cost is 7.[2]

D. RSG

It is 5*5 gate which has five input and five output.

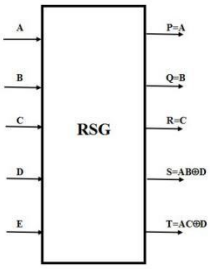

Fig 4. RSG

Inputs for the above gate is 0,A,B,C and Output is P,Q,R,S.Quantum cost is 10.[2]

B.Available fast adders using reversible logic gate:Modular adder based on HNG and PG[1]:

In this modular addition is performed using HNG and PG.HNG gate is used as full adder whereas PG is used as a half adder. The third bit of the half adder is set to zero. The important parameter of any reversible gate is a quantum cost here the quantum cost of PG is 4.

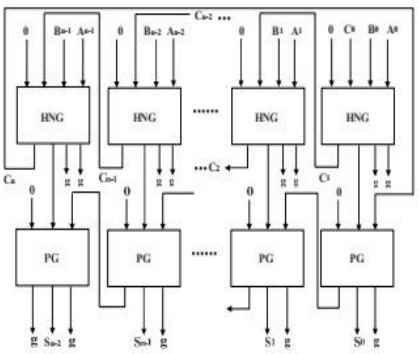

Fig 5. RCA with EAC using HNG an PG gates

The above diagram shows the carry save adder using (HNG, PG)reversible logic gates.HNG is 4*4 gate it has 4 input and 4 output similarly PG is a 3*3 gate and has 3 input and 3 output.one of the input is left unused and set to be zero. Garbage output of HNG and PG are two and three respectively.First, we have to take a number(X) and it's three co-prime number(X1, X2, X3). The modulus operation is done by using the below formula

Y1=X%X1;
Y2=X%X2;
Y3=X%X3;

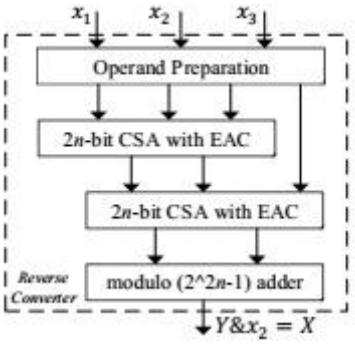

Fig 6. Full reverse converter for the moduli set

As mentioned earlier, the only difference with the division and modulus is that -in division, we take quotient as the result but in modulus, we take the remainder as the result. for example, in division, if 9/4 is given the output will be 2, in modulus the output will be 1. The resultant of modulus operation(Y1, Y2, Y3) is added by CSA using HNG and PG.End around carry is used to avoid missing of carry in an addition[1]. Thus the parallel processing of addition and modulus is done.

III.PROPOSED SYSTEM

A. NOVEL DESIGN OF NRA&RNA - MCRG REVERSIBLE LOGIC GATE:

- NRA gate as full adder:

It is 4*4 gate has 4 input and 4 output and used as full adder shown in fig 7

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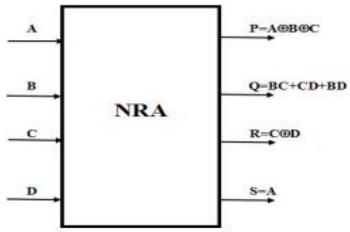

Fig 7. NRA

All four inputs are used. Among four outputs two outputs are considered and others are garbage output.

P=A⊕B⊕C
Q=BC+CD+DB
R=C⊕D
S=A
Here, P represents Sum and Q represents Carry.

The truth table for NRA gate is given table 1

Table I Truthtable for full adder NRA gate

Din	A	B	C	D	P	Q	R	S	D out
00	0	0	0	0	0	0	0	0	00
01	0	0	0	1	0	0	1	0	02
02	0	0	1	0	1	0	1	0	10
03	0	0	1	1	1	1	0	0	12
04	0	1	0	0	1	0	0	0	08
05	0	1	0	1	1	1	1	0	14
06	0	1	1	0	0	1	1	0	06
07	0	1	1	1	0	1	0	0	04
08	1	0	0	0	1	0	0	1	09
09	1	0	0	1	1	0	1	1	11
10	1	0	1	0	0	0	1	1	03
11	1	0	1	1	0	1	0	1	05
12	1	1	0	0	0	0	0	1	01
13	1	1	0	1	0	1	1	1	07
14	1	1	1	0	1	1	1	1	15
15	1	1	1	1	1	1	0	1	13

- NRA gate as Half adder:

It is 4*4 gate has 4 input and 4 output and used as half adder shown in fig 4.2. The above NRA gate can also be used as half adder by assuming B=0.Three inputs(A,C,D) are used.B=0 is the constant input.Among four outputs two outputs(Q, R) are used and others(P, S) are garbage output.

The expressions are changed into
P=A⊕C
Q=CD
R=C⊕D
S=A
R represents Sum and Q represents Carry.

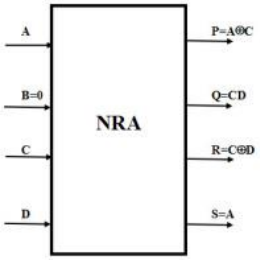

Fig 8. Half adder design of NRA

The truth table for half adder NRA gate is given in table II

Table II Truthtable for Half adder NRA gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	1	0	1	0
0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0
0	1	1	0	1	0	1	0
0	1	1	1	1	1	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	1
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	1
1	1	1	1	0	1	0	1

- RNA gate as full adder:

It is 3*3 gate has 3 input and 3 output and used as full adder shown in fig 4.3.

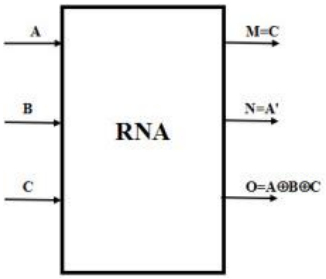

Fig 9. RNA gate

All three inputs are used. Among three outputs only one output(O) is used and others are garbage output.

M=C
N=A
O=A⊕B⊕C
Where O represents Carry.
The truth table for RNA gate is given in table III

Table III Truthtable for RNA gate

Din	A	B	C	M	N	O	D out
0	0	0	0	0	1	0	2
1	0	0	1	1	1	1	7
2	0	1	0	0	1	1	3
3	0	1	1	1	1	0	6
4	1	0	0	0	0	1	1
5	1	0	1	1	0	0	4
6	1	1	0	0	0	0	0
7	1	1	1	1	0	1	5

- Full adder design of MCRG:

MCRG is used as a full adder and is shown in fig 4.1.RNA and NRA gates are combined to form a full adder namely MCRG. The sum is taken from one gate and carry is taken from another gate. The total number of inputs for the MCRG gate is four out of which the first bit of NRA gate is set to be zero. The total number of outputs are seven out of which five are garbage output.

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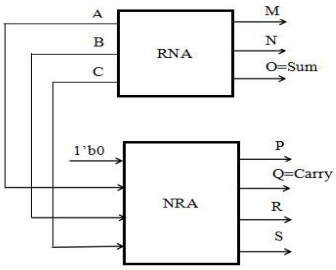

Fig 10. MCR gate

M=$\overline{C}$
N=$\overline{A}$
O=A⊕B⊕C
P=B⊕C
Q=BC+CD+DB
R=C⊕D
S=A
Where O represents Sum and Q represents Carry.

The truth table for MCRG adder is given in table IV

Table IV Truthtable for MCR gate

A	B	C	D	M	N	O	P	Q	R	S
0	0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	0	0
0	1	0	0	0	1	1	1	0	0	0
0	1	0	1	0	1	1	1	1	1	0
0	1	1	0	1	1	0	0	1	1	0
0	1	1	1	1	1	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0	1
1	0	0	1	0	0	1	0	0	1	1
1	0	1	0	1	0	0	1	0	1	1
1	0	1	1	1	0	0	1	1	0	1
1	1	0	0	0	0	0	1	0	0	1
1	1	0	1	0	0	0	1	1	1	1
1	1	1	0	1	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1	0	1

B. Proposed Modular Design based on MCRG

In the proposed RNS modular adder design the parallel computation of addition and modulus is done with three different gates and three different adders to find the best and efficient design for high-speed applications. The block diagram of the proposed modular design is shown in fig 4.14. The output of the modulus operation is given to the carry select adder, carry skip, carry save adder. To perform addition operation we need full adder or half adder. The three gates are used separately with each adder to get the results. Finally, the sum and carry are obtained from each adder. Thus, the RNS operation is successfully completed.

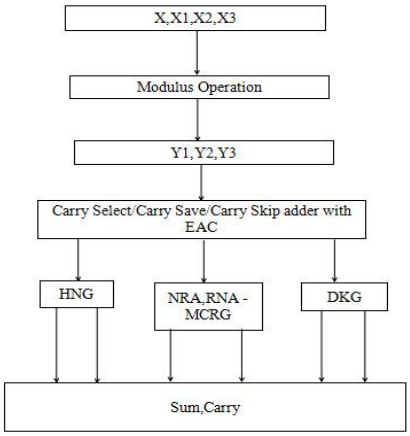

Fig 11. Modular design adder using HNG,DKG and MCRG

V.OUTPUT WAVEFORMS

A. NRA GATE:

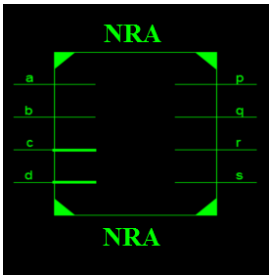

Fig 12. RTL schematic view of NRA

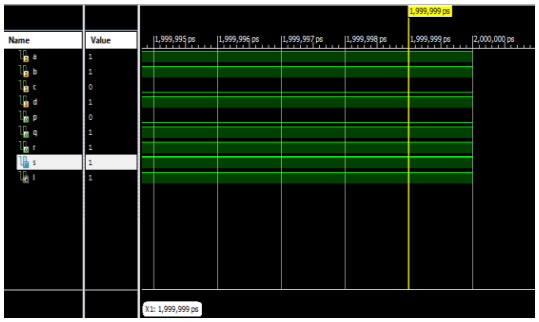

Fig 13. Output of NRA gate

B.RNA GATE

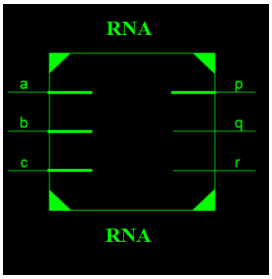

Fig 14. RTL schematic view of RNA

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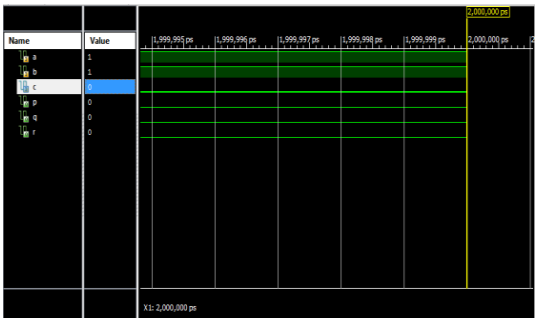

Fig 15. Output of RNA gate

C.COMBINED NRA & RAN -MCRG

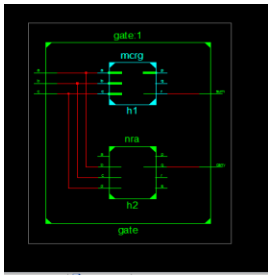

Figure 16 RTL schematic view of MCRG

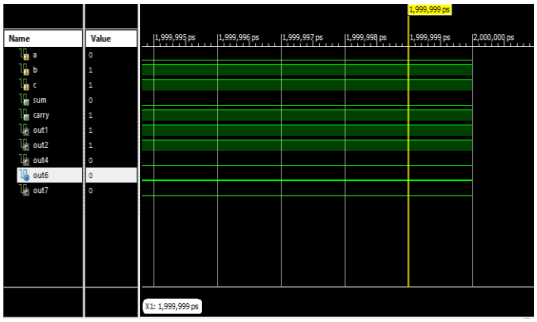

Fig 17. Output of MCR gate

D. *NRA&RAN-MCRG*

i Carry save adder:

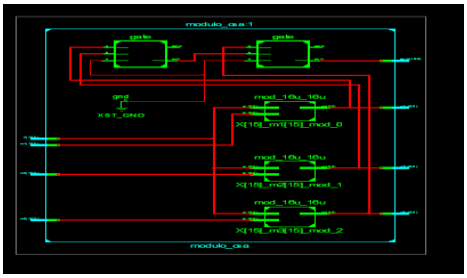

Fig 18. RTL schematic view of MCRG-Carry save adder

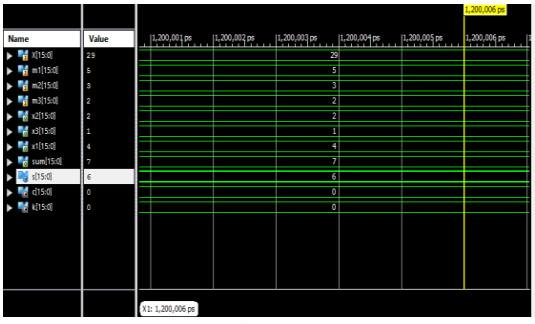

Fig 19. Output of MCRG-Carry save adder

ii Carry select adder:

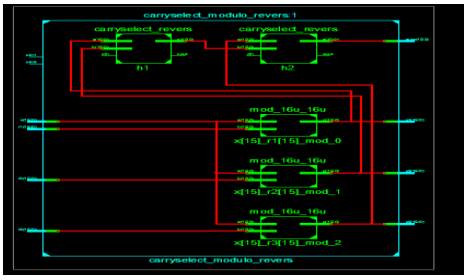

Fig 20. RTL schematic view of MCRG-Carry select adder

Fig 21. Output of MCRG-Carry select adder

iii Carry skip adder:

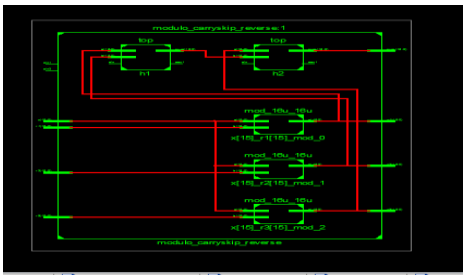

Fig 22. RTL schematic view of MCRG-Carry skip adder

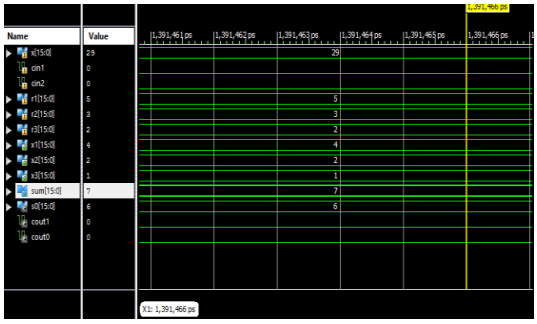

Fig 23. Output of MCRG-Carry skip adder

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E. DKG with full adder

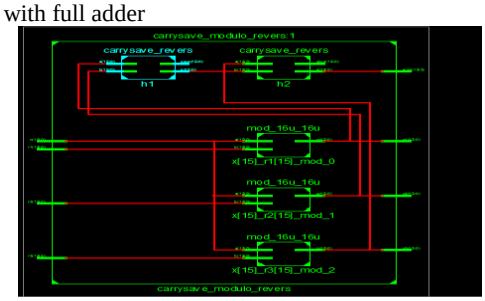

Fig 24. RTL schematic view of DKG full adder

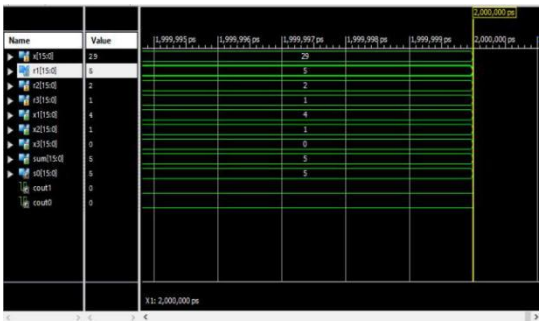

Fig 25. Output of DKG adder

F. HNG with full adder

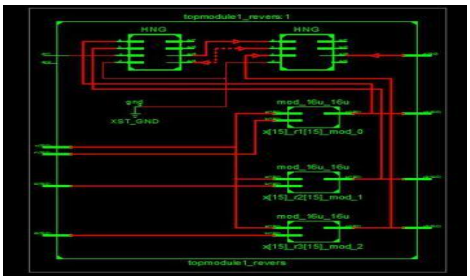

Fig 26. RTL schematic view of HNG adder

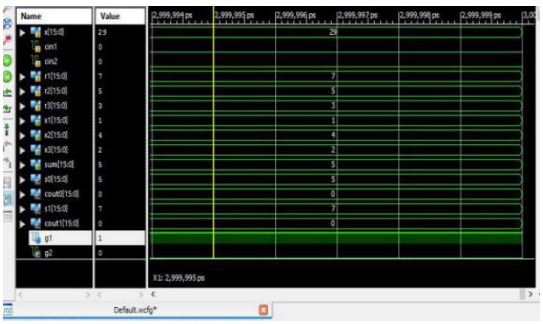

Fig 27. Output of HNG adder

VI.RESULTS AND DISCUSSION

The MCRG(NRA&RNA),HNG and DKG are used with the full adders.

Table V Comparision Table of HNG.DKG and MCRG

Gates	Delay	Power	Area	Quantum Cost
HNG	69.06ns	328.16mv	1282 LUT's	6
DKG	64.788ns	328.22mv	1297 LUT's	-
MCRG	56.188ns	328.22mv	1267 LUT's	-

Power of MCRG gate is less than or equal to all other gates and it is not higher.MCRG power is reduced compared to HNG.NRA&RNA has reduced delay,area and power compared to all other gates.

VII.CONCLUSION

In this paper, we have discussed the novel design of MCRG-NRA&RNA gates and its functions. Three reversible logic gates such as HNG, DKG, and MCRG gates are separately used with other full adders to perform parallel computations such as modulus and addition. The outputs of these gates are compared with the other gates to find out the efficient one. The simulation is carried out using the Xilinx tool 14.5 From the results and discussion, we have evidence that MCR gate is the best compared to other gates in terms of area, power, and delay.

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