A Novel Approach for Low leakage, High performance Universal Gate Implementation in Deep Submicron Regime using subthreshold Leakage Control Techniques

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Abstract: **The rapid progress in semiconductor technology have led the feature sizes of transistor to be shrunk, there by evolution of Deep Sub-Micron (DSM) technology; there by the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-operated electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers have to be realized with very low power requirements. Leakage power consumption is one of the major technical problem in DSM regime in CMOS VLSI circuit design. A comprehensive study and analysis of various leakage power minimization techniques have been presented in this paper. A proposed novel Leakage reduction technique is developed with the combination of stack with sleepy keeper approach using two input NAND gate with Low & High threshold voltage (Vth). The results are simulated using Microwind Software tool. This proposed technique reduces the power dissipation, power delay, power delay product (PDP) and circuits with improved performance.**

Keywords: Leakage Power, Deep sub-micron Regime, High Vth, Low Vth, sleepy keeper, sleepy stack, PDP.

1. INTRODUCTION

The increasing demand for portable electronic appliances has triggered numerous research efforts in low power VLSI circuit design. Power dissipation is becoming widely recognized as a top-priority issue in VLSI circuit design. One of the most challenging problems faced by the VLSI designer in present scenario, is to find out new and effective circuit design techniques to reduce the overall power dissipation without compromising the performance of the device.

Power dissipation in VLSI circuits can be broadly divided into two categories: Dynamic or switching power, and Static or leakage power dissipations. Dynamic power dissipation results due to charging and discharging of internal capacitances in the circuit. Leakage power dissipation occurs during the static input state of the device. Leakage power dissipation is much more noticeable in low threshold voltage MOS transistors. This power dissipation arises because of the presence of subthreshold and gate oxide leakage currents. Gate oxide leakage current occurs because of the desire to increase the performance characteristics of MOS transistor by decreasing the thickness of the gate oxide layer while subthreshold leakage current occurs between the source and the drain region of a MOS transistor in weak inversion state. The subthreshold leakage current occurs even when the applied gate voltage-V_{GS}, is less than the threshold voltage-V_{TH}, of the MOS transistor. A general formula for the total power dissipation in a VLSI circuit can be expressed as [1]

$$P_T = P_{dynamic} + P_{static} \quad (1)$$

$$P_T = \alpha C V_{DD}^2 f_{clk} + N(1-\alpha) V_{DD} I_S + N(1-\alpha) V_{DD} I_{ox}. \quad (2)$$

where α is the switching activity factor which represents the probability of the output switching, C is the sum of all load capacitance in the design, V_{DD} is the supply voltage, f_{clk} is the clock frequency, N is the number of gates, I_S is the average subthreshold leakage current of a gate, and I_{OX} is the average thinoxide leakage current of a gate.

Subthreshold leakage current is the main component of leakage power dissipation in VLSI circuits in Deep Submicron and nanoscale technologies. Hence P_T may be approximated as

$$P_T = \alpha C V_{DD}^2 f_{clk} + N(1-\alpha) V_{DD} I_S. \quad (3)$$

The organization of this paper is as follows: Section-2 describes various types of subthreshold leakage reduction techniques to reduce the leakage current. Section-3 presents the proposed technique called sleepy keeper with stacking of the transistor with High threshold voltage (Vth) & Low threshold voltage (Vth). Section-4, presents simulation results using Microwind software tool. Finally the conclusion is presented in section-5.

2. SUBTHRESHOLD LEAKAGE POWER REDUCTION TECHNIQUES

Fig. 1 [2] shows that subthreshold leakage current or power is the most dominant leakage component in short channel MOS transistors. This leakage current is caused by the

inability to completely turn off a MOS transistor. In long channel MOS transistors, the threshold voltage is considered as the boundary between the cutoff and active inversion region. However, in short channel MOS transistor, this boundary is not abrupt and the transistor conducts even in weak inversion region when, V_{GS} is less than the threshold voltage of the MOS transistor.

Fig. 2. shows the flow of subthreshold leakage current when the applied gate voltage-V_{GS}, is less than the threshold voltage-V_{TH}, of an nMOS transistor.

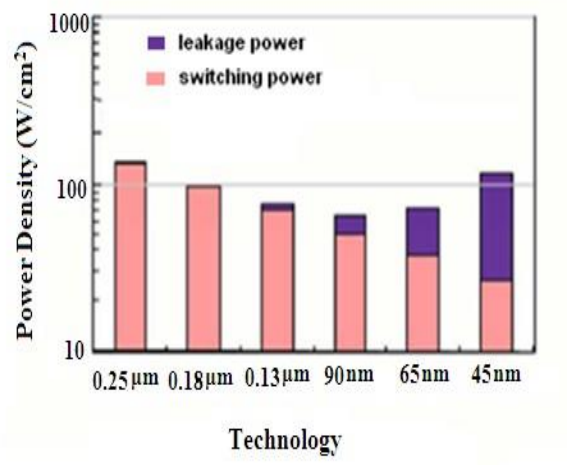

Fig. 1. *Leakage Vs Switching power dissipation trends*

According to BSIM4 MOSFET model, the equation governing this subthreshold leakage current can be expressed as [3]

$$I_{SB} = I_0 \exp\{(V_{GS} - V_{TH0} - \eta V_{DS} + \gamma V_{SB}) / nV_T\}$$

$$\{1- \exp(-V_{DS}/V_T)\} \quad (4)$$

Where

$$I_0 = \mu C_{OX} (W/L) V_T^{\,2} e^{1.8} \quad (5)$$

$$V_T = KT/q \quad (6)$$

here V_{GS}, V_{DS} and V_{SB} are the gate to source, drain to source, and source to bulk voltages respectively of a MOS transistor, μ denotes the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W and L denote the width and length of the channel of the transistor, K is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of an electron, V_T is the thermal voltage, V_{TH0} is the zero biased threshold voltage, γ is body effect coefficient, η denotes the drain induced barrier lowering coefficient, and n is the subthreshold swing coefficient.

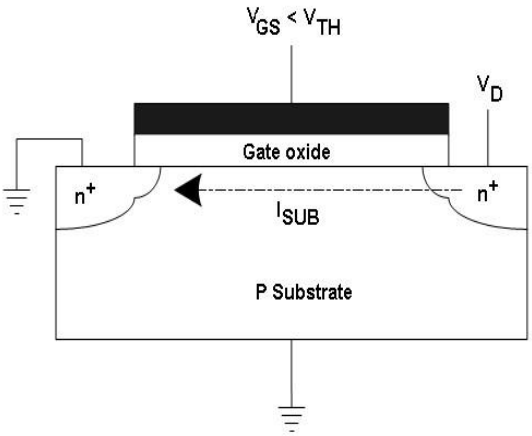

Fig. 2. *Subthreshold leakage current in an nMOS transistor*

It is evident from (2) that the subthreshold leakage current is a strong function of the threshold voltage of a MOS transistor. This leakage current is highly undesirable in a digital circuit in deep submicron (DSM) and nanoscale technologies. Fig. 3 [4] shows the subthreshold leakage power dissipation trends according to the International Technology Roadmap for Semiconductors.

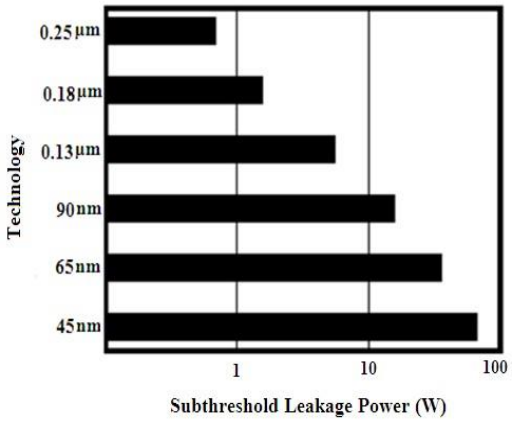

Fig. 3. *Subthreshold leakage power dissipation trends*

In order to reduce power dissipation in digital circuits, its supply voltage is scaled down. However, with the reduction in the supply voltage, circuit propagation delay increases. In order to reduce this increase in the propagation delay, threshold voltage of the MOS transistor is reduced. The reduction in the threshold voltage leads to increase in subthreshold leakage current in short channel MOS transistors. This leakage current is the most dominant source of leakage power dissipation in deep submicron and nanoscale technologies.

Subthreshold leakage current increases exponentially with the decrease in the threshold voltage of the MOS transistor. So, increasing the threshold voltage of the transistor is an effective way to reduce subthreshold leakage current. Portable battery operated systems such as mobile phones and PDAs, that remain idle for most of the times, are severely affected by this leakage power loss.

Different existing subthreshold leakage power reduction techniques are explained further.

2.1 Base Approach

Fig. 4. shows the block diagram of a digital circuit using conventional CMOS transistors. In this approach, pull up network is designed using pMOS transistors and pull down network by nMOS transistors. Pull up network is connected to the power supply, VDD while the pull down network is connected to the ground, GND.

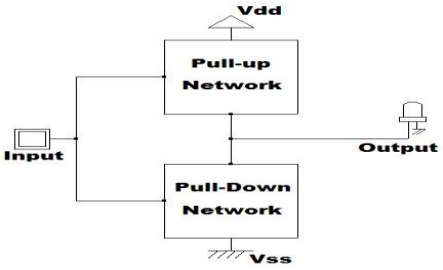

Fig. 4. *Base Approach*

2.2. Sleep Approach

Sleep approach is used for reduction of gate oxide and sub threshold leakage current in DSM technology [5]. Sleep approach is used to cut off the circuit from V_{dd} to ground, so we insert a PMOS transistor above pull-up network and V_{dd} and NMOS transistor below pull-down Network and GND [6]. Sleep transistors of high threshold voltages are used in this technique. Fig. 5. Shows this structure. During active mode, sleep transistors are on (s=0 and s'=1) and the circuit is operating normally. Whereas during standby mode these sleep transistors turn off (s=1 and s'=0) and disconnect the circuit from power supply V_{dd} and ground. Thus minimizes the leakage power efficiently and increases the performance of the circuit [9].

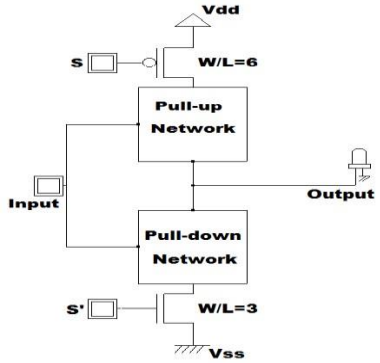

Fig. 5. *Sleep Approach*

2.3. Stack Approach

Another technique for leakage power reduction is the force stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [7]. Figure 6 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach combines the sleep and stack approaches.

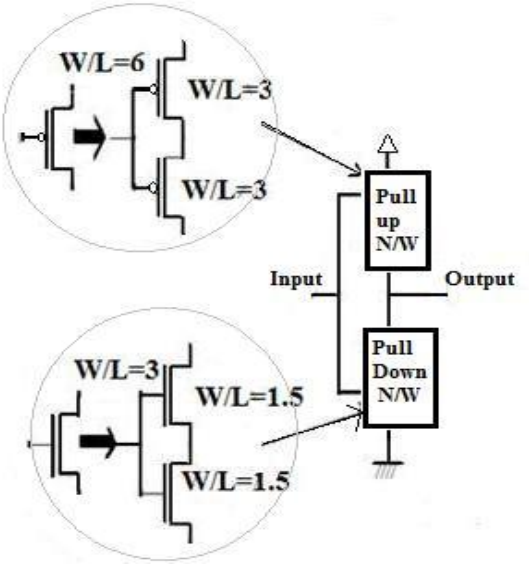

Fig. 6. *Stack Approach*

2.4. Sleepy Keeper Approach

The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to Vdd and NMOS transistors connect to Gnd. It is well known that PMOS transistors are not efficient at passing Gnd similarly, it is well known that NMOS transistors are not efficient at passing Vdd. However, to maintain a value of '1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of 1 and an NMOS transistor connected to Vdd to maintain output value equal to '1' when in sleep mode, as shown in Fig. 7.

An additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects Vdd to the pull-up network. When in sleep mode, this NMOS transistor is the only source of Vdd to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of '0' in sleep mode, given that the '0' value has already been calculated, the sleepy keeper approach uses this output value of '0' and a PMOS transistor connected to Gnd to maintain output value equal to '0' when in sleep mode.

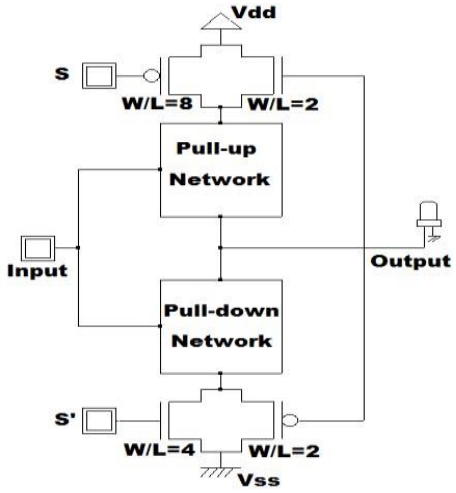

Fig.7. *Sleepy Keeper Approach*

2.5 Sleepy Stack Approach

The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors [7]. Figure 5 shows its structure. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S‟, which are sleep signals.

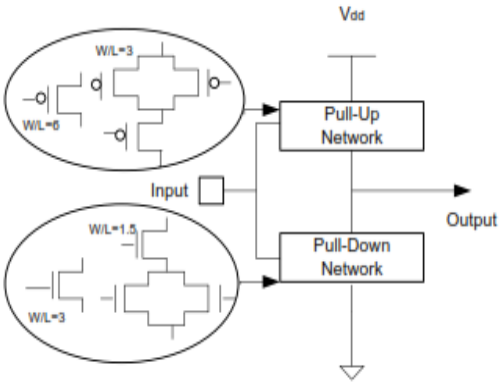

Fig.8. *Sleepy Stack Approach*

3. PROPOSED TECHNIQUE - Modified Sleepy Keeper with Stacking of the Transistor with High V_{th} & Low V_{th} Transistor.

In this section, we discuss the structure and operation of the proposed high-performance, low-leakage design using stack with sleepy keeper approach. The proposed circuit is compared with well-known previous approaches, i.e., Basic NAND Gate, Sleep transistor with Low and high V_{th}, Forced Stacking, Sleepy Keeper and Sleepy Stack. Firstly we discuss the operation of proposed NAND gate circuits (P1, P2 in parallel and N1, N2 in series combination) with low and high V_{th} transistors (N3, P5) as shown in fig. 9 and 10. In standby mode, both the sleep transistors of pull up and pull down network are off, i.e. transistor P3, P4 and N4, N5 are off. We do so by making S1=1 and S2=0. A working of the NAND gate is similar to the inverter, we use four transistors, two PMOS as pull up and two NMOS as pull down. The output of the NAND gate is one when any one of the input vector is low or zero. In proposed approach we incorporate the stack approach with sleepy keeper approach for optimizing the leakage power in the circuit and thus improves the performance of the circuit by applying unique technique for leakage reduction.

In Proposed approach, we combined two techniques i.e., stack approach and sleepy keeper approach, to reduce the leakage power consumption in the circuit. Here we use two NMOS in pull down network (N4, N5) and two PMOS in pull up network (P4, P5), so as to provide the stacking of the transistor for further leakage reduction. To maintain the proper logic level ‘1’ we insert NMOS transistor (N3) parallel to PMOS stacked transistors in pull up network, to connect sleep transistor to V_{dd} to the pull up network. In sleep mode, this NMOS transistor connects V_{dd} to the pull up network when sleep transistor cut off.

Similar action also repeat in pull down network the two NMOS transistor provide the stacking effect. To maintain the value ‘0’ in sleep mode a PMOS transistor is connected in parallel with two NMOS transistors. To maintain an output value to ‘0’ PMOS transistor (P5) is connected to GND in sleep mode. For Proper Logic, NMOS is connected to V_{dd} and PMOS is connected to GND. The stacking of the transistor reduces the leakage power in proposed approach and enhances the performance of the circuit by maintaining proper logic of the circuit.

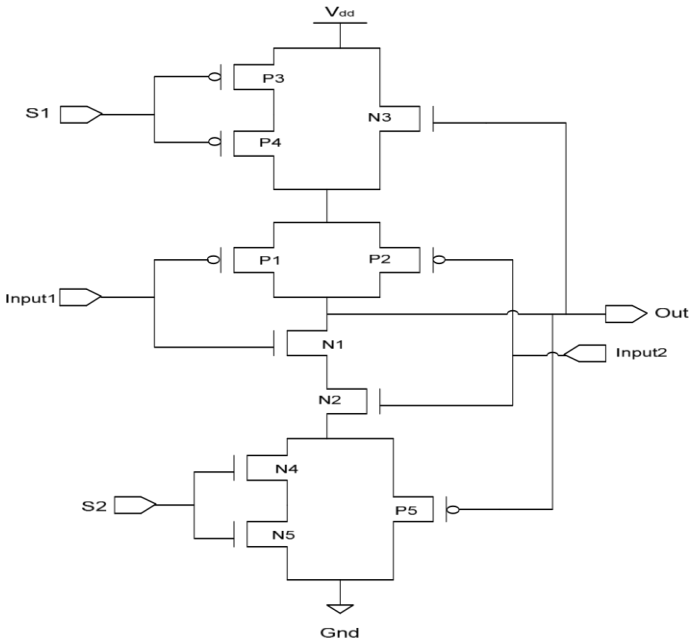

Fig. 9. *Proposed technique with Low V_{th} transistors*

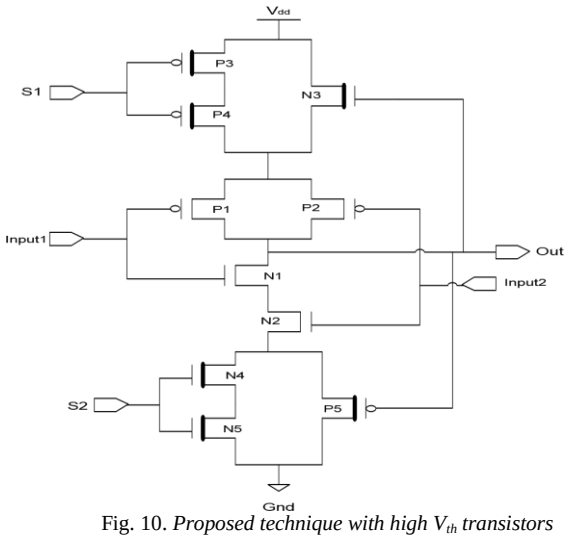

Fig. 10. *Proposed technique with high V_{th} transistors*

4. SIMULATION RESULTS

A 2 input NAND gate is simulated with leakage power reduction techniques like sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS. After analysing the results in terms of average power consumption, static power consumption, delay and PDP we conclude that proposed circuit with DTCMOS is producing comparatively better results. All schematics are designed and simulated using Microwind EDA tool for a two input NAND gate using BSIM4 MOSFET model with 45nm technology. Performance characteristics such as static power dissipation, dynamic power dissipation, propagation delay and power delay products in static and dynamic conditions were observed using conventional CMOS, Sleep, Stack, Sleepy keeper and sleepy stack techniques at a temperature of 27 ^{0}C and a Supply voltage, V_{DD} of 1.1V.

Table 2 shows all possible static input combinations for measuring static power dissipation in a two input NAND gate. Fig. 11 shows the waveform to measure the dynamic power dissipation in the logic gate using conventional CMOS and stack techniques. Similarly Fig. 12 shows the waveform to measure the dynamic power dissipation in the two input NAND gate using sleep and sleepy keeper techniques.

Static power dissipation was obtained by combining all possible static input combinations. The overall static power dissipation was calculated as the average of power dissipation in all possible static input combinations. In the case of Sleepy Keeper technique, Sleep and high V_{TH} transistors were turned OFF when the sleep signal was activated while they were turned ON when the sleep signal was deactivated. This static power was measured for 50 ns time interval.

Dynamic power dissipation was obtained by applying two dynamic clock inputs A and B of same frequency of 200 MHz and at a temperature of 27 ^{0}C. The supply voltage, V_{DD} was fixed at 1.1 V. In the case of Sleepy Keeper technique, sleep and high V_{TH} transistors were turned ON during the measurement of dynamic power dissipation. This power dissipation was also measured for 50 ns time interval.

Propagation delay of the logic gate was measured from the trigger input edge reaching 50 % of V_{DD} to the circuit output edge reaching 50 % of V_{DD}. Power delay product is measured to determine the efficiency of a circuit in terms of both power dissipation and propagation delay. Power delay product of a digital circuit is the product of its power dissipation and its propagation delay. Static and dynamic power delay products were obtained for the logic gate using various techniques.

Table-1: Comparison of Power, Delay, PDP & Static Power of sleep, forced stack, sleepy keeper and sleepy stack & Proposed Circuit with low V_{th} and high V_{th} NMOS and PMOS transistors.

Technique	**P_{avg} (uW)**	**Delay (ns), t_p**	**PDP (fs) = P_{avg} * t_p**	**Static Power (ns)**
Base case NAND Gate	1.532	3.70	5.668	107.2
Forced stacking	2.49	9.76	24.30	7.869
Sleep Transistor with Low Vth	1.255	6.917	8.680	5.287
Sleep Transistor with High Vth	1.614	3.99	6.43	1.23
Sleepy Keeper	2.094	35.65	74.65	1.467
Proposed Circuit with Low Vth	1.081	.028	0.0302	1.032
Proposed Circuit with High Vth	.921	.081	.0746	.8149

Table-2: Static input combinations for measuring static power dissipation

Static input A	Static input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

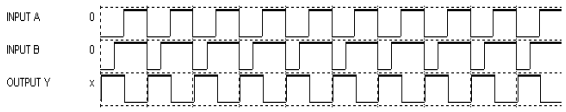

Fig. 11: *Waveform to measure the dynamic power dissipation using conventional CMOS and Stack techniques*

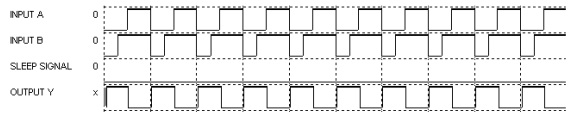

Fig. 12: *Waveform to measure the dynamic power dissipation using sleep and sleepy keeper techniques*

5. CONCLUSION

Performance characteristics such as static power dissipation, dynamic power dissipation, propagation delay and power delay products in static and dynamic conditions of a two input NAND gates were analyzed using various techniques. Performance characteristics of the logic gate were compared using conventional CMOS, Sleep, Stack, Sleepy keeper and sleepy stack techniques in 65 nm technology.

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this paper, we present a new circuit structure named "stacking with sleepy keeper Approach" to tackle the leakage problem. The Stacking with sleepy keeper Approach with DTCMOS has a combined structure of four well-known low-leakage techniques, which are the forced stack, sleep transistor techniques, DTCMOS. However, unlike the forced stack technique & the sleepy Keeper over technique can utilize high-V_{th} transistors without incurring large delay overhead. Also, unlike the sleep transistor technique, the combination of stack approach with sleepy keeper approach retain exact logic state and mitigate leakage power. In future new approach of leakage reduction technique at gate level and block level are expected to give more power saving than the existing approach at CMOS circuit level design.

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