

A Nine Level Diode Clamped Inverter Based Three Level Boost Converter with Fuzzy Logic Controller

Mr. R.Gandhi M.E.,(Ph.D)
Head of the department / EEE
Gnanamani college of engineering
Namakkal, India

Mr. G.Mahendran M.E
Department of EEE
Gnanamani college of engineering
Namakkal, India.

Abstract— In this paper active front-end solution to balance the dc-link capacitor voltage of the nine-level diode clamped inverter. Capacitor voltage balancing is performed by a three-level boost converter connected to the two inner capacitors of a nine-level diode-clamped inverter and additional balancing circuits at the other two outer capacitors. The load power factor conditions at a high modulation index. And the reliability of the dc-link capacitor voltage at the desired level. The TLBC has advantages in high power applications to reduced switching losses and reduced reverse recovery losses of the diode. With reduced inductor current ripple in TLBC, a smaller size inductor can be used in TLBC compared to the conventional boost converter. A fuzzy control system is a control system based on fuzzy logic a mathematical system that analyzes analog input values in terms of logical variables that take on continuous values between 0 and 1, in contrast to classical or digital logic, which operates on discrete values of either 1 or 0 (true or false, respectively).

Keywords— TLBC, modulation index, switching losses, reverse recovery losses.

I. INTRODUCTION

Three highly popular voltage-source multilevel inverters can be divided into three categories according to their topology: neutral point clamped, flying capacitor, and cascade H-bridge. Studies on three-, four-, five- and six-level diode-clamped inverters for such use like static VAR compensators, high voltage grid interconnections, and variable speed motor drives have been considered. It has long been recognized that, for the diode-clamped inverter with more than three levels, a passive front-end capacitor voltage balancing method is only achievable if the modulation index is limited to about 60% of its maximum value for loads with a typical 0.8 power factor. If the modulation index is increased more than this value, the center capacitors gradually discharge the inverter output converges at three levels.

To overcome this limitation, a multilevel inverter can be supplied by isolated dc sources such as external circuit as the active front-end solution of dc-link capacitor balancing, using balancing circuit by transferring charge from one capacitor to another capacitor to equilibrium level or the modification of the pulse width modulation (PWM) switching pattern. Many authors proposed PWM strategies for capacitor voltage balancing to avoid extra cost when using active front-end or balancing circuit. This method is found to have limitation on the range of operation with the changing of the power factor and modulation index.

Once a PWM strategy is employed for dc-link capacitor voltage balancing, solving problems such as total harmonic distortion, common-mode voltage cancellation, and leakage current elimination with the same strategy is not feasible. It has been pointed out in the introduction of that capacitor voltage balancing and common mode voltage cancellation cannot be achieved concurrently in a multilevel inverter. In photovoltaic (PV) power systems, a conventional two level inverter is supplied by the series connection of PV arrays (PVAs). Partial shading, dust, and disparity in panel aging (yellowing) cause differences in the V - I characteristic of the PV string.

The differences result to the rise of several local maximum power points in the string P - V curve that leads to the reduction of the power generated from its potential maximum. It is more practical to install PV with fewer series connections and more on parallel connection. Some authors proposed a substitution of the conventional two level inverter by a multilevel inverter.

The series of independently controlled PVAs placed parallel to every dc link capacitor. By using this configuration, the n-level inverter will need n - 1 sets of PVAs. In this paper, a three-level boost converter (TLBC) is used to supply a five-level diode-clamped inverter.

In energy conversion system, a boost chopper is often used due to its simple topology and control method. The TLBC has advantages in high power applications such as reduced switching losses and reduced reverse recovery losses of the diode. With reduced inductor current ripple in TLBC, a smaller size inductor can be used in TLBC compared to the conventional boost converter.

DC-link capacitor voltage balancing is performed using a combination of active front-end and balancing circuits. TLBC is used to balance the two inner capacitors, C1 and C2, and another balancing circuit is used to balance the outer capacitors, C1 and C4, by transferring the charge from the inner capacitors to the outer capacitors. The prototype is tested for various load power factor conditions to evaluate its performance at a high modulation index.

The PID controller algorithm involves three separate constant parameters, and is accordingly sometimes called three-term control: the proportional, the integral and derivative values, denoted P, I, and D. Simply put, these values can be interpreted in terms of time: P depends on the present error, I on the accumulation of past errors, and D is a prediction of future errors, based on current rate of change.

The weighted sum of these three actions is used to adjust the process via a control element such as the position of a control valve, a damper, or the power supplied to a heating element.

In the absence of knowledge of the underlying process, a PID controller has historically been considered to be the best controller. By tuning the three parameters in the PID controller algorithm, the controller can provide control action designed for specific process requirements. The response of the controller can be described in terms of the responsiveness of the controller to an error, the degree to which the controller overshoots the set point, and the degree of system oscillation.

The use of the PID algorithm for control does not guarantee optimal control of the system or system stability. A fuzzy control system is a control system based on fuzzy logic a mathematical system that analyzes analog input values in terms of logical variables that take on continuous values between 0 and 1, in contrast to classical or digital logic, which operates on discrete values of either 1 or 0 (true or false, respectively). Fuzzy controllers are very simple conceptually. They consist of an input stage, a processing stage, and an output stage.

The input stage maps sensor or other inputs, such as switches and so on. The appropriate membership functions and truth values. The processing stage invokes each appropriate rule and generates a result for each, then combines the results of the rules. Finally, the output stage converts the combined result back into a specific control output value. That output value is very accurate compare to PID Controller.

II. CIRCUIT DIAGRAM

A. CIRCUIT DIAGRAM OF THE PROJECT

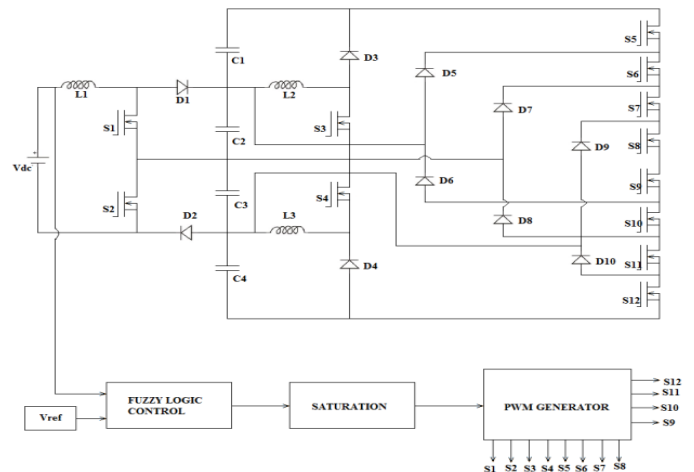


Figure 1 Circuit Diagram

The TLBC has advantages in high power applications such as reduced switching losses and reduced reverse recovery losses of the diode. With reduced inductor current ripple in TLBC, a smaller size inductor can be used in TLBC compared to the conventional boost converter.

DC-link capacitor voltage balancing is performed using a combination of active front-end and balancing circuits. TLBC is used to balance the two inner capacitors, C1 and C2, and another balancing circuit is used to balance the outer capacitors, C1 and C4, by transferring the charge from the inner capacitors to the outer capacitors. The proposed configuration is suitable for a grid-connected PV system which operates in unidirectional power flow.

B. OPERATING CONDITIONS

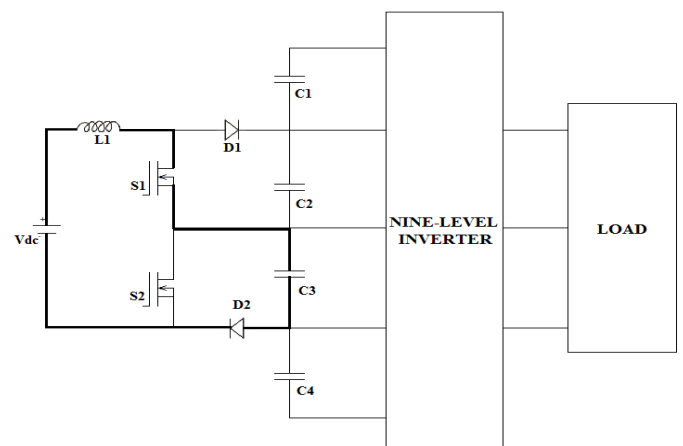


Figure 2 Inner Capacitor Balancing using boost TL Chopper

The switching signal waveforms and inductor current i_L s for duty ratios ($D < 0.5$). From t_0 to t_1 , S1 is on, and S2 is off; moreover, the inductance current flows in the circuit marked with thick solid lines. The energy is stored in the inductance, capacitor C3 is charged, and V_{c3} gradually rises.

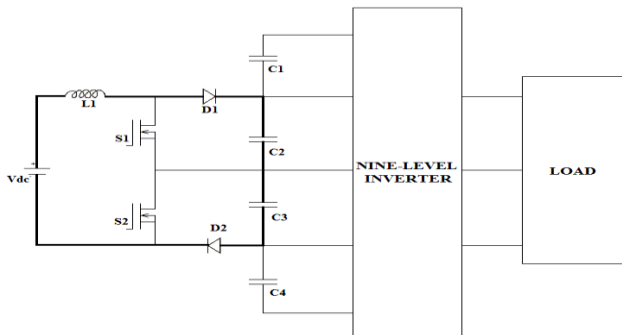


Figure 3 Inner Capacitor Balancing using boost TL Chopper

From t_1 to t_2 and t_3 to t_4 , S1 and S2 are off, and current flow is marked. The energy stored in the inductance is transferred to C2 and C3.

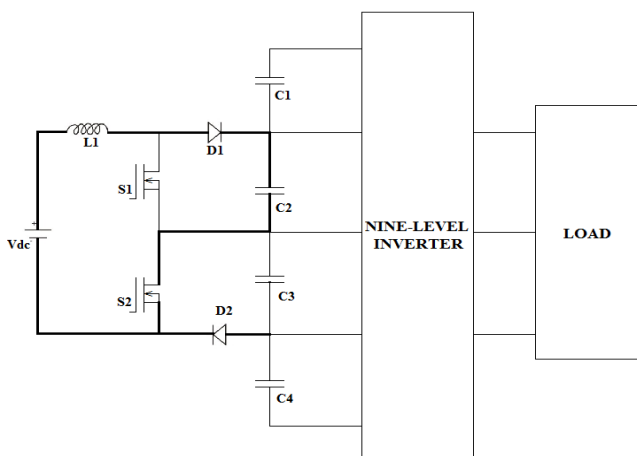


Figure 4 Inner Capacitor Balancing using boost TL Chopper

From t_2 to t_3 , S1 is off, and S2 is on. The inductance current flows in the circuit marked. The energy is stored in inductance, capacitor C2 is charged, and V_{c2} gradually rises.

III. SIMULATION RESULTS

A. SIMULATION DESIGN

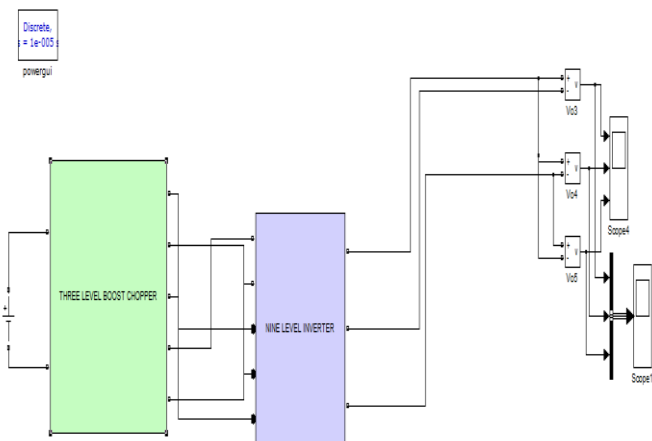


Figure 5 Circuit Diagram

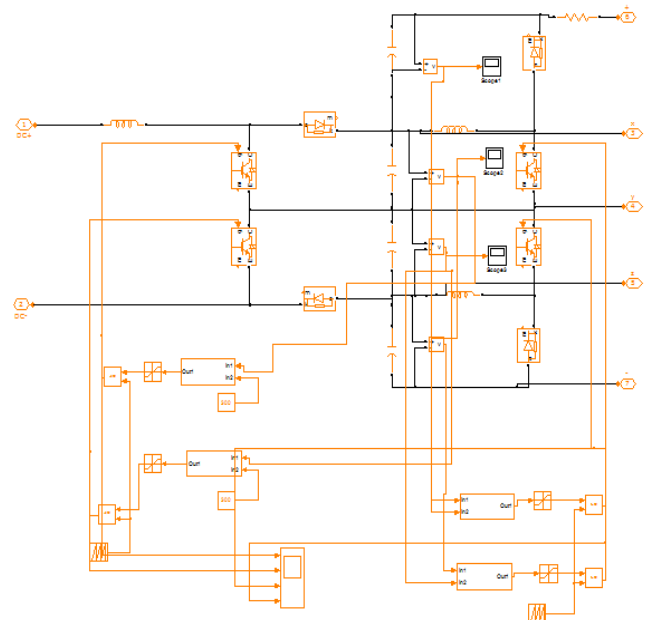


Figure 6 Three Level Boost Chopper

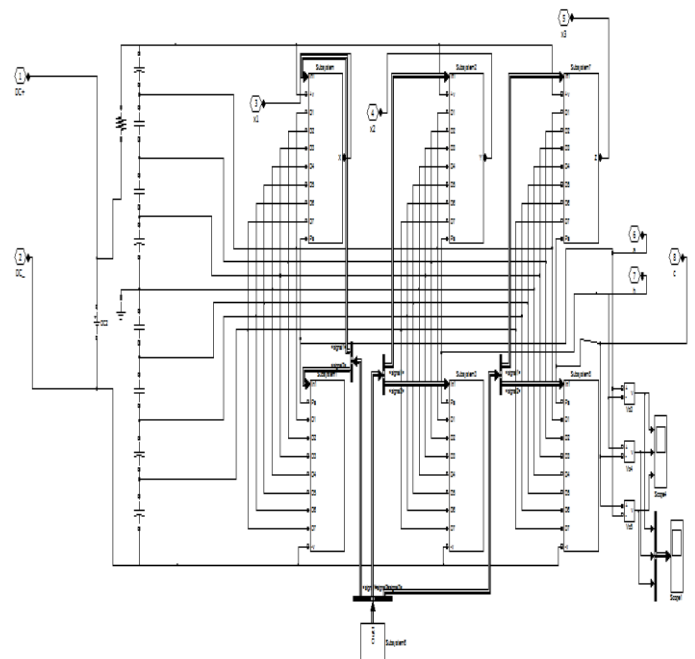


Figure 7 Nine Level Inverter

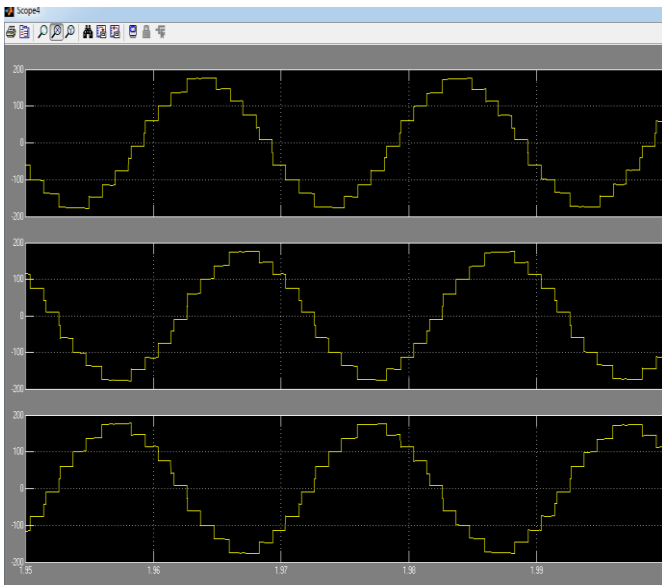


Figure 8 Single Phase Nine level output

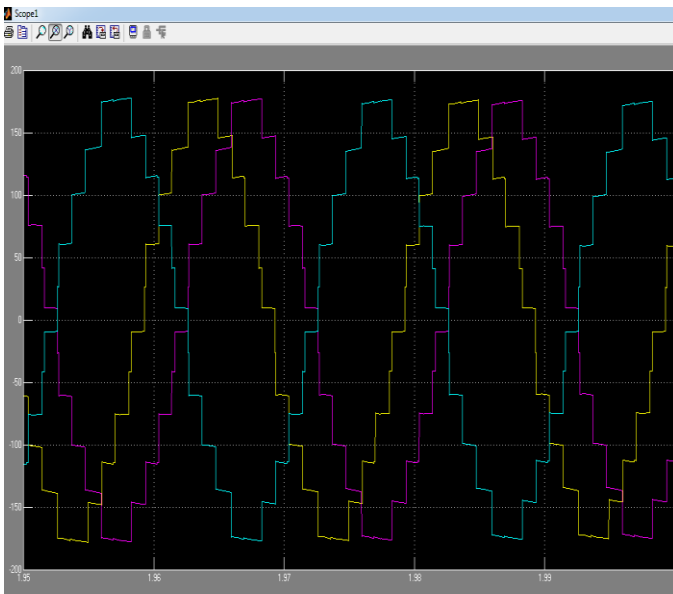


Figure 9 Three Phase nine Multiple output

IV. CONCLUSION

The new configuration to balance the dc-link capacitor voltages of the Nine-level diode-clamped inverter. Connecting a TLBC at the input of the inverter regulates the two inner dc-link capacitors' voltage at the desired level with the changing of the converter dc source and, at the same time, provides voltage balancing. The dc-link capacitor balancing performance is not affected by the changing of the load power factor, even though the inverter has operated at a high modulation index. Balancing circuits are added to balance the voltage of the two outer capacitors. The investigations show that the proposed converter operates well in various load power factor conditions. Rules can be solved in parallel in hardware, or sequentially in

software. The results of all the rules that have fired are "defuzzified" to a crisp value by one of several methods. There are dozens, in theory, each with various advantages.

V. ACKNOWLEDGMENT

At the outset, I express my heartfelt gratitude to **PARENTS** and **GOD**, who has been my strength to bring this project to light.

At this pleasing moment of having successfully completed my project, I wish to convey my sincere thanks and gratitude to our beloved Chairman **Dr.T.ARANGANNAL** and beloved Chairperson **Smt.P.MALALEENA**, **GNANAMANI EDUCATIONAL INSTITUTIONS, PACHAL**. Who have provided all the facilities to me.

I would like to express my sincere thanks to our Chief Executive Officer **Mr.K.VIVEKANANDAN** and our Administrative Officer **Dr.P.PREMKUMAR**, **GNANAMANI EDUCATIONAL INSTITUTIONS, PACHAL** for their support to bring the best in me.

I would like to convey my sincere thanks to our Principal **Dr.V.BASKARAN**, **GNANAMANI COLLEGE OF ENGINEERING, PACHAL** for forwarding us to do my project and offering adequate duration in completing my project.

I expand sincere thanks to our Head of the Department **Mr. R.GANDHI**, and to my Project Guide **Mr. R.GANDHI, M.E.,(Ph.D.)**, Head of the Department/ EEE, **GNANAMANI COLLEGE OF ENGINEERING, PACHAL** for her kind guidance and encouragement during this project.

I would also like to express my thanks to all the Staff members of my department, friends who helped us directly and indirectly in all aspects of the project work to get completed successfully.

REFERENCES

- [1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.
- [2] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static VAR compensation," in *Conf. Rec. IEEE IAS Annu. Meeting*, 1994, vol. 2, pp. 921–928.
- [3] M. Marchesoni and M. Mazzucchelli, "Multilevel converters for high power ac drives: A review," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1993, pp. 38–43.
- [4] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.
- [5] B. A. Welchko, "A three-level MOSFET inverter for low-power drives," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 669–674, Jun. 2004.
- [6] A. Bendre, S. Krstic, J. Vander Meer, and G. Venkataraman, "Comparative evaluation of modulation algorithms for neutral-point-clamped

- converters,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 634–643, Mar./Apr. 2005.
- [7] N. Hatti, Y. Kondo, and H. Akagi, “Five-level diode-clamped PWM converters connected back-to-back for motor drives,” *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1268–1276, Jul./Aug. 2008.
- [8] N. Hatti, K. Hasegawa, and H. Akagi, “A 6.6-kV transformerless motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers,” *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 796–803, Mar. 2009.
- [9] M. M. Renge and H. M. Suryawanshi, “Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives,” *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1598–1607, Jul. 2008.