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# A New Topology For A Single Phase 21 Level Multi Level Inverter Using Reduced Number Of Switches

Mr.JITHIN.J.I
PG STUDENT, EEE Dept., KARUNYA UNIVERSITY
COIMBATORE, TAMILNADU

Mr.A.BENUEL SATHISH RAJ
ASSISTANT PROFESSOR EEE Dept., KARUNYA UNIVERSITY, COIMBATORE.TAMILNADU

***Abstract*—The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. To synthesize maximum levels at the output voltage, the proposed topology is optimized for various objectives, such as the minimization of the number of switches, gate driver circuits and capacitors, and blocking voltage on switches. This new type of converter is suitable for high voltage and high power applications. This multilevel inverter has ability to synthesize waveforms with better harmonics spectrum. The power loss in the circuit is less due to less number of switches. There are numerous topologies has been introduced and widely studied for utility and drive application. In this work a study of 21-level inverter using less number of switches as compare to the technologies previously developed. MATLAB software is used for simulate the 11-level inverter. Multilevel inverter is fulfilling the requirement of heavy-duty electric and hybrid-electric vehicles (EH's) of large electric drives (>250KW). When we increases the level of inverter then we gets the high output voltage and the stress of each switch is also reduces means each switches faces low value of dv/dt. The output waveform of multilevel inverter follows the sinusoidal waveform hence the harmonic contents are less. Therefore there is small loss of energy in the circuit if we study the cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches.**

**The objective of this paper is to make the easy cheap and good multilevel inverter with less number of switches and understanding the working and simulation of a 21-level with the proposed converter topology using less number of switches by PWM technique using MATLAB/SIMULINK software**

***Keywords- MATLAB Simulink; 21- level inverter; Modulation Technique***

## I . INTRODUCTION

The voltage source inverters produce a voltage or a current with levels either 0 or ±V dc they are known as two level inverters. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various pulse width modulation (PWM) strategies. In high power and high voltage applications, these two level inverters, however, have some limitations in operating at high frequency mainly due to switching devices should be used in such a manner as to avoid problems associated with their series- parallel combinations that are necessary to obtain capability of handling high voltages and currents. It may be easier to produce a high power, high voltage inverter with the multi-level structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverters without requiring higher ratings on the individual devices can increase the power rating. The unique structure of Multi-level voltages sources inverters allow them to reach high voltages with low harmonics without the use of transformer or series connected synchronized switching devices. As the number of voltage levels increases, the harmonic content of output voltage waveform decreases significantly.

## II. EXISTING BASIC TOPOLOGIES

The general structure of multi-level converter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically from capacitor voltage sources. As number of levels increases, the synthesized output waveform has more steps, which provides a staircase wave that approaches a desired waveform. Also, as steps are added to waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of voltage levels increases. The Multi-level inverters can be classified into three types. [1]– [4]

- Diode-clamped or neutral point clamped topology(NPC)

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- Capacitor clamped or flying capacitor clamped topology
- Cascaded H-bridge topology

*a)DIODE- CLAMPED MULTI – LEVEL INVERTER*

A diode – clamped (m-level) inverter (DCMLI) as shown in Fig.1 typically consists of (m-1) capacitor on the dc bus and produces m levels on the phase voltages. Figure shows full bridge five-level diode clamped converter. The numbering order of the switches is Sa1, Sa2, Sa3, Sa4, S'a1, S'a2, S'a3, S'a4. The dc bus voltage consists of four capacitors C1, C2, C3, and C4. For a dc voltage $V_{dc}$, the voltage across each capacitor is $V_{dc}/4$, and each devices voltage stress is limited to one capacitor voltage level V dc/4 through clamping diodes. An m-level inverter leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1) X (m-1) clamping diodes. [5]

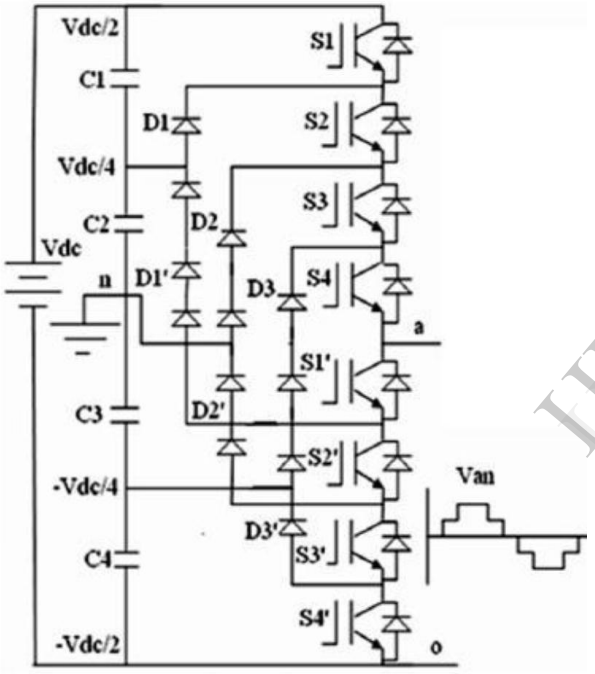


Fig.1. Single phase Diode clamped inverter

The main drawbacks of NPC topology are their unequal voltage sharing among series connected capacitors that result in dc-link capacitor unbalancing and requiring a great number of clamping diodes for higher levels.

*b)FLYING CAPACITOR MULTILEVEL INVERTER*

The figure 2 shows a single phase full bridge 5-level inverter based on flying capacitors. Each phase like has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of the capacitors indicates the voltage level between calming points. All phase legs share the DC link capacitors C1 to C4. [6]

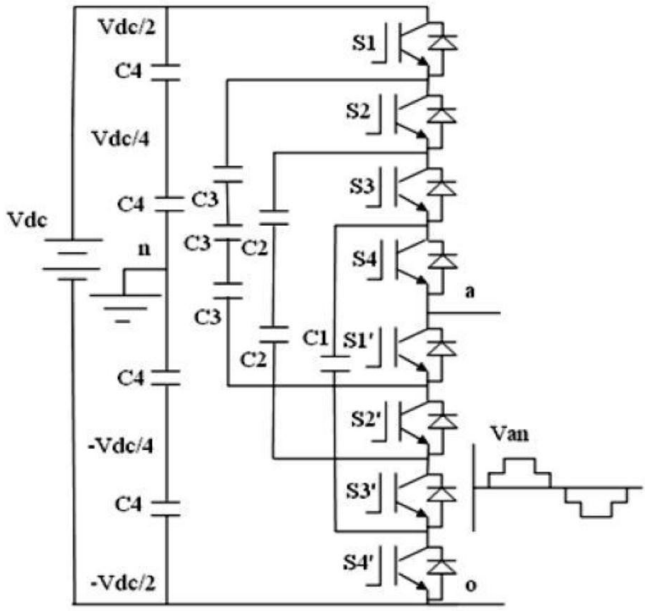


Fig.2. single phase flying capacitor inverter

The FC multilevel converter uses flying capacitor as clamping devices. These topologies have several attractive properties in comparison with the NPC converter, including the advantage of the transformer less operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductor switches [8], [9]. But, these converters require an excessive number of storage capacitors for higher voltage steps.

*c)CASCADED MULTI-LEVEL INVERTER*

A relatively new converter structure called Cascaded Multi-level inverter, can avoid extra clamping diodes or voltage balancing capacitors. The converter topology used here is based on the series connection of single phase inverters with separate DC sources .The different topologies by which h-bridge are designed are

*Cascaded H-bridge:* Figure 2.3 shows the basic block of cascade H-bridge Multi-level inverter and its associated switching instants. As shown it consists of four power devices and a DC source. The switching states for four power devices are constant i.e., When S1 is on, S2 cannot be on and vice versa. Similarly with S3 and S4.

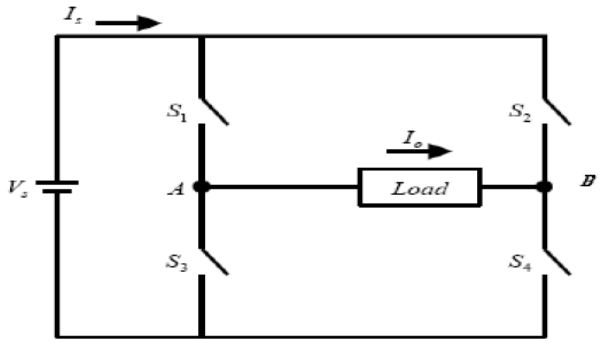


Fig.3. Block of a H-bridge Multi-level inverter

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Figure 4 shows the power circuit for one phase of multi-level inverter. The resulting voltage ranges from +3Vdc to -3Vdc and the staircase are nearly sinusoidal, even without filtering.

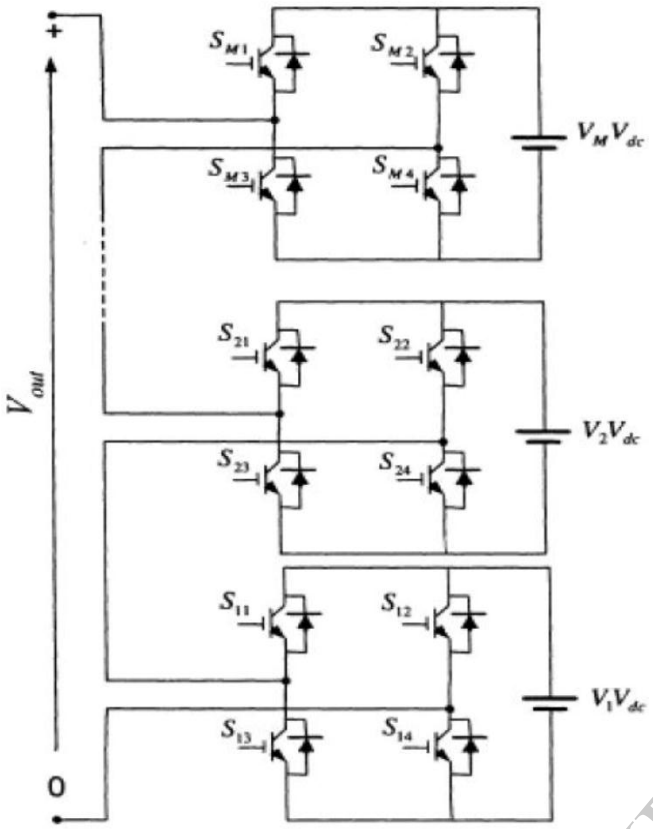


Fig .4.Circuit diagram of 4-level cascade multi-level inverter

*Hybrid H-bridge:* A hybrid H-bridge inverter consists of a series of H-bridge inverter units. The general function of this Multi-level inverter is to synthesize a desired voltage form several DC sources (SDCSs). Each SDCS is connected to an H-bridge inverter. The AC terminal voltages of different level inverters are connected in series. Unlike diode clamp or flying capacitors inverters the hybrid H-bridge inverter does not require any voltage clamping diodes or voltage-balancing capacitors.

Hybrid multilevel converters have been presented in [12], [13]. In the hybrid topologies, the dc voltage sources magnitudes are unequal or changed dynamically [14]. These converters reduce the size and cost of the converter and improve the reliability since less number of semiconductors and capacitors are used in this topology [15]. The hybrid multilevel converters comprises of different multilevel topologies which are having unequal values of dc voltage sources and different modulation techniques [12]. With appropriate selection of switching devices, the converter cost is significantly reduced. But, the application of different multilevel topologies result in loss of modularity and produces problems with switching frequency and restrictions on the modulation and control method [16].

## III. PROPOSED TOPOLOGY

Multilevel voltage source inverter is recognized as an important alternative to the normal two level voltage source inverter especially in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter.

The proposed converter consists of less number of switches when compared to the other familiar topologies. The initial cost reduces because of the switch reduction. So, it looks attractive and an apt one for industrial applications.

The general circuit diagram of the proposed multilevel inverter is shown in the figure 5. The switches are arranged in the manner as shown in the figure. For the proposed topology, we just need to add only one switch for every increase in levels, so initial cost gets reduced. Let us see operation in the next subdivision in detail for the 21-level inverter as shown in Fig.6

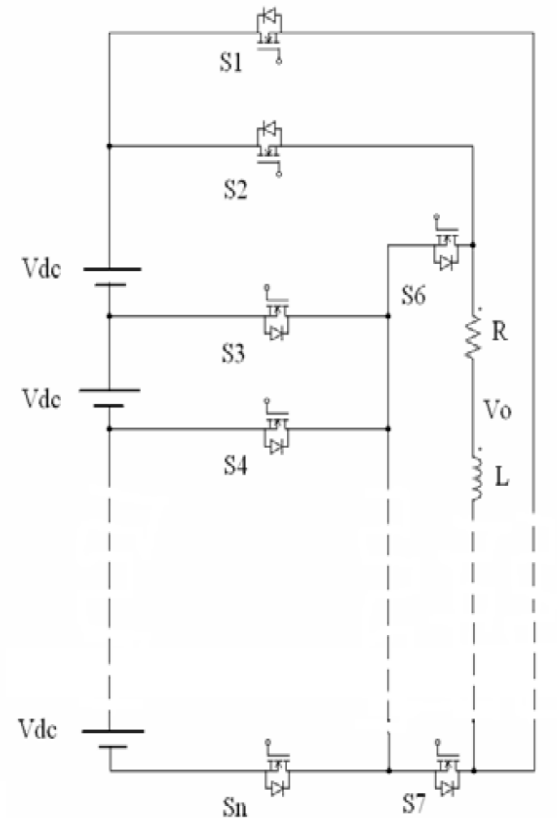


Fig.5. General Circuit Diagram of the Proposed Multilevel Inverter Topology

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## IV .PROPOSED TOPOLOGY DESIGN AND ANALYSIS

Simulation results are shown here by the help of MATLAB/Simulink for proposed 21-level inverter in fig 6. The results are shown by PWM control technique. The battery of 22 volts DC each is chosen for input supply. The load of industries is generally R-L load hence the load connected here is the same R-L load. The IGBTs are used in this topology for higher stability of the circuit.

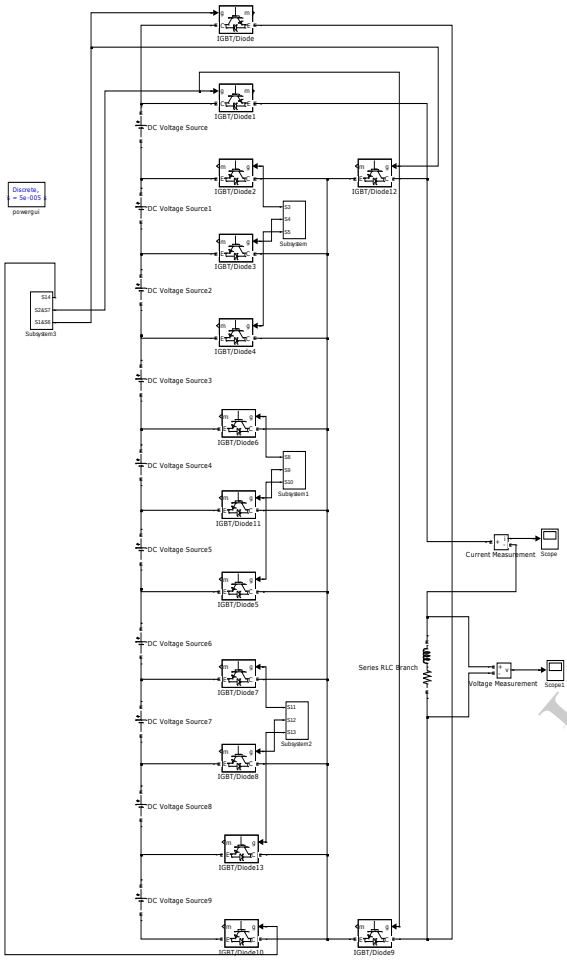

Fig.6. MATLAB/Simulink circuit for proposed 21-level inverter

## V .FIRING CIRCUIT FOR PWM TECHNIQUES

DC voltages are compared with different types of triangular waves to obtain the gate pulses. The relational operators are used. The pulse width of the pulses required determines the value of the constants. Pulse width is determined by the on time of each switch and these signals are used for switching the IGBTs. There are four subsystems in this circuit. The outputs from the comparison operational amplifiers are compared with high frequency square waves and given to AND gate for obtaining the PWM pulses. These signals are used as the gating signals for the switches. The below table shows the various different switching states in this proposed topology.

| S.NO | Conducting Switches | Output Voltage |
|---|---|---|
| 1 | S2,S7,S3 | $+V_{DC}$ |
| 2 | S2,S7,S4 | $+2V_{DC}$ |
| 3 | S2,S7,S5 | $+3V_{DC}$ |
| 4 | S2,S7,S8 | $+4V_{DC}$ |
| 5 | S2,S7,S9 | $+5V_{DC}$ |
| 6 | S2,S7,S10 | $+6V_{DC}$ |
| 7 | S2,S7,S11 | $+7V_{DC}$ |
| 8 | S2,S7,S12 | $+8V_{DC}$ |
| 9 | S2,S7,S13 | $+9V_{DC}$ |
| 10 | S2,S7,S14 | $+10V_{DC}$ |
| 11 | NIL | 0 |
| 12 | S1,S6,S3 | $-V_{DC}$ |
| 13 | S1,S6,S4 | $-2V_{DC}$ |
| 14 | S1,S6,S5 | $-3V_{DC}$ |
| 15 | S1,S6,S8 | $-4V_{DC}$ |
| 16 | S1,S6,S9 | $-5V_{DC}$ |
| 17 | S1,S6,S10 | $-6V_{DC}$ |
| 18 | S1,S6,S11 | $-7V_{DC}$ |
| 19 | S1,S6,S12 | $-8V_{DC}$ |
| 20 | S1,S6,S13 | $-9V_{DC}$ |
| 21 | S1,S6,S14 | $-10V_{DC}$ |

Table I

Values of $V_{DC}$ for different switching states are as shown in Table I. The firing pulses from the four subsystems are shown in Fig.7.These pulses are given to the proposed 21-level multilevel inverter.

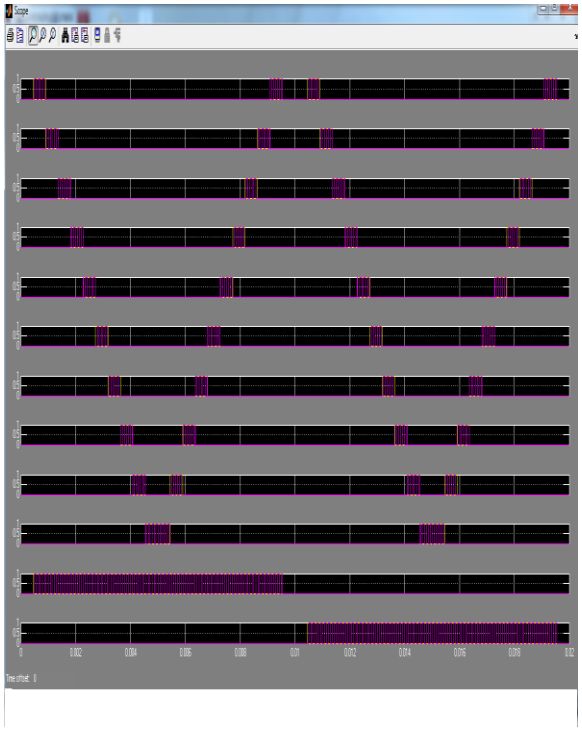

Fig.7.PWM firing pulses

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## VI.RESULTS AND FUTURE SCOPE

To evaluate the performance of the proposed multilevel converter topology in the generation of desired output voltage staircase waveform, a single-phase 21-level multilevel is simulated and tested. The main objective of this proposed topology is to synthesis the output voltage with minimizes error with respected to the reference voltage. It is important to note that the calculation of optimal switching angles so as to obtain selective harmonic elimination and minimize the total harmonic elimination is not the objective of this work.

In the experimental point of view, the output voltage waveform and the output current waveform are studied and analyzed. Regarding this, the converter has been adjusted to produce a 50 Hz, 21-level staircase waveform. In this experiment the load is a series R-L load(R=20Ω and L=75mH).The results of this are shown in Fig.8. & Fig.9.

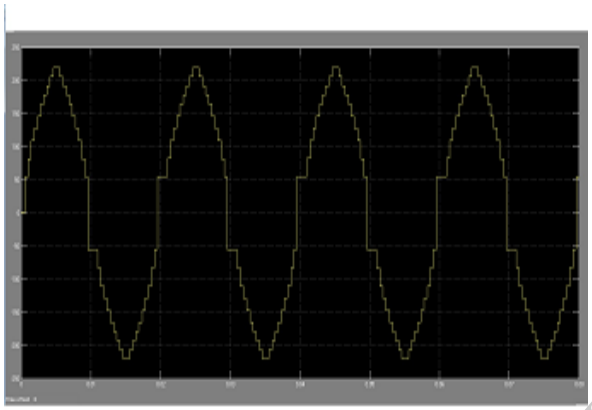

Fig.8.Output voltage waveform

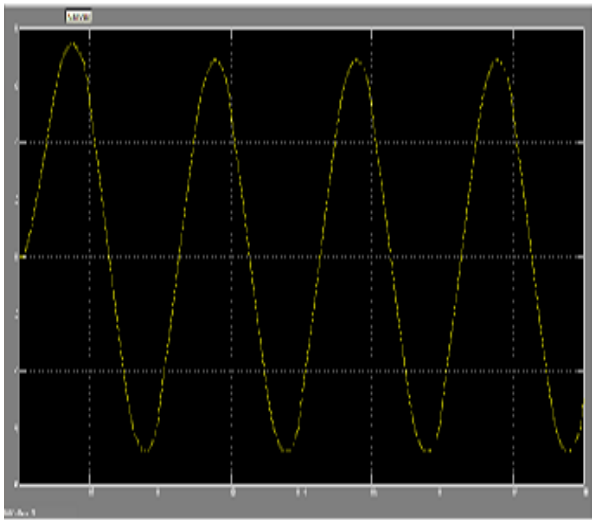

Fig.9.Output current waveform

## VII.FUTURE SCOPE

The main drawback to be considered in this proposed topology is that it requires multiple numbers of Dc sources. This could be resolved by integrating DC-Dc converters in the input side of the proposed topology. Thus by using a single DC source and DC-DC converters, the same output could be obtained as obtained by using multiple DC sources in this work.

Also several PV panels could be used for each levels of the inverter to obtain the desired output. But this requires voltage balancing between each level. To generate desired output with best power quality waveform, the number of voltage steps should be increased or another appropriate switching technique could be used.

## VIII.CONCLUSION

The simulation of 21-level multilevel inverter is successfully done using PWM technique. The main limitation of this topology is that the upper two batteries of the circuit are being used for more time compared to other batteries and hence those two batteries of the inverter discharge rapidly compared to other sources in the circuit. Another feature is that the upper two switches have higher rating than the other switches providing unequal switching devices rating. However the number of switches reduces considerably as the number of levels in the output increases.

| INVERTER TYPE | 5-LEVEL | 7-LEVEL | 9-LEVEL | 11-LEVEL |
|---|---|---|---|---|
| CASCADED H BRIDGE | 8 | 12 | 16 | 20 |
| PROPOSED TOPOLOGY | 6 | 7 | 8 | 9 |
| % REDUCTION | 25% | 41.7% | 50% | 55% |

Table II

A comparison between the cascaded topology and proposed topology is shown in Table II which clearly shows the percentage reduction in the number of switching devices as the number of output level increases.

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