Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 01, January-2016

A Multiprocessor System on Chip for Real Time Cardiac Monitoring

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***Abstract*— This paper proposes an approach to design a Multi Processor System on Chip (MPSoC) based on the state of the art Field Programmable Gate Array (FPGA). It is possible to embed more than one processor in single chip with the dense architecture of FPGAs. Here the development of the embedded system put forward by considering a case study in the biomedical field. Using this design approach we can develop an SoC for Real Time Cardiac Monitoring. The system is designed using Zynq processing system from the Vivado design suite by Xilinx. The dual core ARM cortex A9 is used with each Zynq processing system. Three CPU cores are used in the proposed system, such that one master and two slaves. One slave is responsible for Human Machine Interface (HMI) and the other slave deals with the database required for different cardiac conditions. The AXI stream bus is used for the inter processor communication. The implementation can be done in Zynq Evaluation and Development (ZED) board.**

***Index Terms*— FPGA, MPSoC, ARM cortex A9, Biomedical field, Human Machine Interface (HMI), Database, AXI stream bus, Zynq Evaluation and Development (ZED) board**

I. Introduction

A Field Programmable Gate Array (FPGA) is a Programmable Logic Device (PLD) that allows high performance data processing because of its high density nature. It is possible to embed one or more processor on the single chip. Moreover we can add other functional devices too this chip. So we can develop Multi Processor System on Chip (MPSoC) [1] in advanced embedded systems. In this way, the processors work with lower frequencies, reducing power consumption without affecting the overall system performance. The application test of this MPSoC deals with the cardiac monitoring based on the electrocardiogram signal (ECG). The electrocardiogram or ECG is today used worldwide as a relatively simple way of diagnosing heart conditions. An electrocardiogram is a recording of the small electric waves being generated during heart activity. We are proceeding by referring ECG of different cardiac conditions.

II. HUMAN MACHINE INTERFACE

The proposed system requires a human machine interface which makes the communication between human and system real. A Human Machine Interface (HMI) is any device or method that will give some idea about current situation of patient under observation. Large number of HMI is used in medical field to have an error free diagnosis of various diseases. We need to monitor the real time cardiac conditions and work on it. So the verily available electrocardiogram so called ECG [2] is used. The electrocardiogram or ECG is today used worldwide as a relatively simple way of diagnosing heart conditions. An electrocardiogram is a recording of the small electric waves being generated during heart activity. The standard ECG provides 12 different vector views of the heart's electrical activity as reflected by electrical potential differences between positive and negative electrodes placed on the limbs and chest wall. As illustrated by the Fig. 1, the ECG is characterized mainly by 5 waves reflecting the activity of the heart during a cardiac cycle (R-R interval); these waves are called P, Q, R, S and T; the Q, R, and S waves are treated as a single composite wave known as the QRS complex. The ECG signal is typically characterized by maximum amplitude of 1 mV and a bandwidth of 0.05 Hz to 100 Hz when we interpret an ECG we compare it instantaneously with the normal ECG and normal variants stored in our memory.

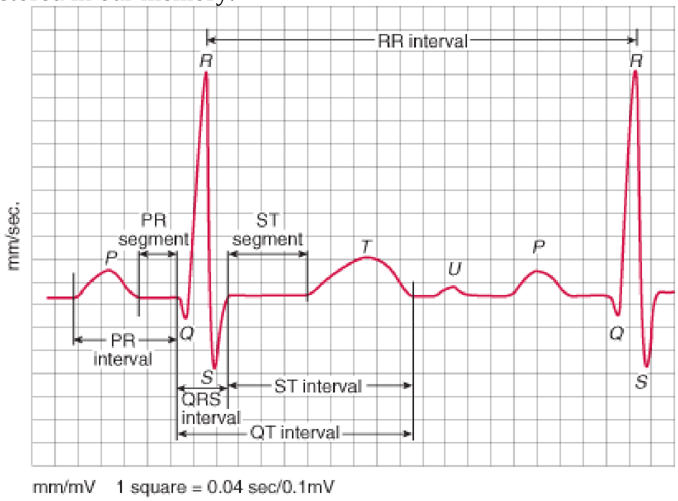

Fig. 1. Typical ECG of a healthy person

III. SYSTEM OVERVIEW

It is a regular practice nowadays; building an entire system on a single chip. We can add many functional devices to SoC. If we add more than one processor to the simple SoC it is then called Multi Processor System on Chip (MPSoC). The proposed system requires 3 processors in a single chip to coordinate different functionalities. In the previous works MicroBlaze [3] processors were used. FSL buses are used for inter processor communication. With a perfect coordination and to some extent, they digitize and process the ECG signal. But the poor quality of IP cores kills most of the developing time. MicroBlaze also has some architectural limitations such as absence of MMU and inability to handle atomic instructions. To surmount these disadvantages we can use ARM cortex A9.

By replacing ARM cortex A9 we can use AXI bus for communication which is far better than FSL used in MicroBlaze. AXI is part of ARM AMBA, a family of micro controller buses. We are recommending AXI-4 bus for high-performance memory-mapped requirements. As illustrated by the Fig. 2, the proposed system contains three CPU cores, such that one master and two slaves.

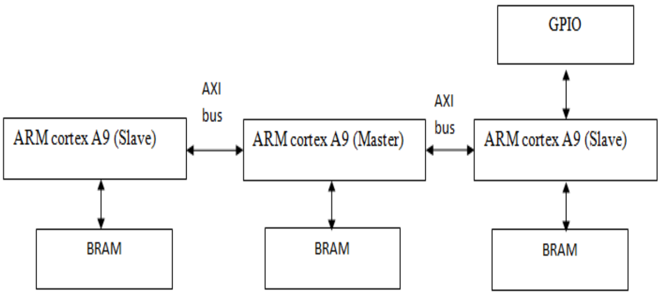

Fig. 2. Basic Block Diagram

One slave deals with capturing real time ECG. It contains General Purpose Input Output (GPIO) to have a Human Machine Interface (HMI). Another slave stores the database of various cardiac conditions. It is preloaded with reference to ECGs made with the help of some Matlab simulations. The master is responsible for entire control and coordination of the system. Each block is associated with some memory block. The inter processor communication is made with AXI stream bus. The implementation can be done in Zynq Evaluation and Development (ZED) board.

IV. HARDWARE AND SOFTWARE DESCRIPTION

As described above, the system is implemented in reconfigurable circuit, that is, FPGA [4] representing the strong actual trend for embedded systems designing. Large number of inbuilt intellectual property (IP) cores and their numerous configurations is possible.

A. Used Development Tools:

The Xilinx FPGA and Zynq SoC [5] devices are extremely flexible and so there is a lot of functionality in the toolset, which is spread across different applications. We are using top level design environment for the hardware design. This tool used to create the contents of the Programmable Logic, and to create the embedded processor section of the design. We will use Vivado to configure our settings for the Zynq “Processing System” section of the design. Xilinx SDK is the tool for software engineers, allowing us to develop C code, generate BSP (Board Support Package)s, and test their code using the debugger

B. Hardware Architecture

The hardware design is created using Vivado 2015.1. The Fig. 3 shows the Master-Slave architecture of our hardware implementation that is a common scenario in embedded systems, where there is a set of real-time and non real-time tasks. Thus, the system uses a star network topology in which each slave processor is connected to the master central processor. This way, a slave processor (A1) is dedicated to perform the real-time tasks, i.e. the ECG analog signal acquiring and some digital processing; a second slave processor (A2) is responsible for HMI tasks; finally, the third processor (A3) that is the master, monitors and coordinates the 2 slaves [6]. It is worth noting that the 3 processors are clocked with the same clock

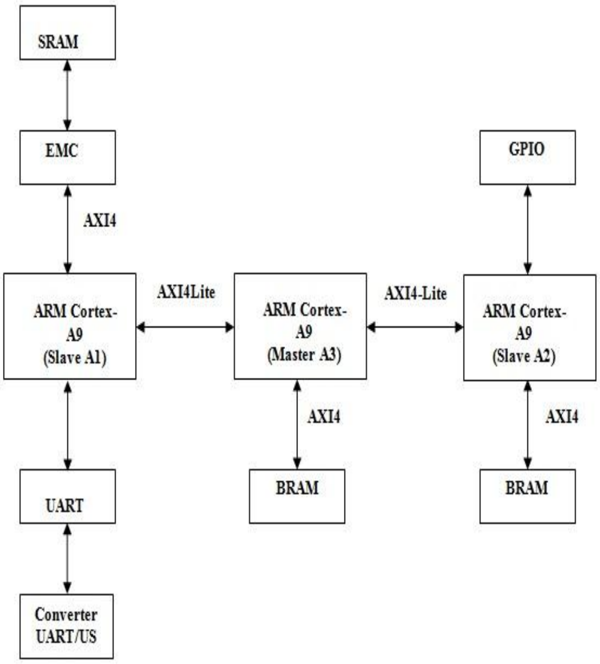

Fig. 3. Architecture of our hardware implementation

The architecture contains the following combination of systems:

i. *Processors bus interfaces:*

The figure 3 depicts the different buses used to interconnect the various design elements: (1).The AXI4 Bus [7] provides single-cycle access to on-chip RAM for each processor. (2).The AXI4-Lite bus acts as means for communication between the 3processors

ii. *Processor A1:*

The first slave processor (A1) architecture consists of the main following IPs cores: (1).The ARM Cortex-A9 is the central processing unit (CPU) of the partial architecture. (2).EMC (External Memory Controller) is the interface for on-board SRAM, which will be used for storing program and data when these latter exceed the BRAM capacity. (3).UART (Universal asynchronous Receiver Transmitter) is the IP core allowing serial communication with a PC (COM port), via an UART/USB converter.

iii. *Processor A2:*

The second slave processor consists of the following IP cores: (1).The processor ARM Cortex-A9 IP core. (2).On-chip dual-port block RAM (BRAM) stores processor's program instructions and data. (3).General Purpose Input Output (GPIO) is used to communicate with simple machine human interface (MHI) that consists of switches.

iv. *Processor A3:*

It is composed only of the 2 basic necessary IPs cores, i.e. the processor ARM Cortex-A9 (A3) and its associated BRAM.

C. Software Architecture

Development of multiprocessor systems are encouraged by use of modern tools available in Computer Aided Development tools like SDK. Thus, an application is broken into small pieces (soft or hard) more easy to manage; each part deals with certain aspect of the application. In our case, it was a system with 3 hardcore ARM Cortex processors. Thus, the software application consists of 3 programs coded in C language, one program by processor. The application software is a C code written in the Xilinx SDK "standalone" environment. Each specific processor program begins naturally by achieving the necessary initializations. Processor A1 handles the database of ECG signal. Processor A2 makes the HMI with the help of GPIO and the values are stored in BRAM. As a master the processor A3 controls and coordinates the 2 slaves A1 and A2. The QRS complex of the ECG signal is the reference point for almost all the ECG applications. In this system the required reference signals are pre-created using Matlab and saved as database in the memory of slave A1. The slave A2 performs the real-time cardiac monitoring and stores the values. A comparison of the live obtained value is done with the signals in the database.

V. EVALUATION

The proposed system can be realized by using the advanced Zynq Processing System. We cannot see much works done in MPSoC using Zynq. Hence this is a novel approach in this field. . Combining the diagnosing properties of ECG in an MPSoC will be a great contribution to the medical field. The communication between processors and other peripherals is expected to be done through AXI4 bus. The system should be able to monitor real time cardiac conditions and compare it with the database and make some predictions about the diseases.

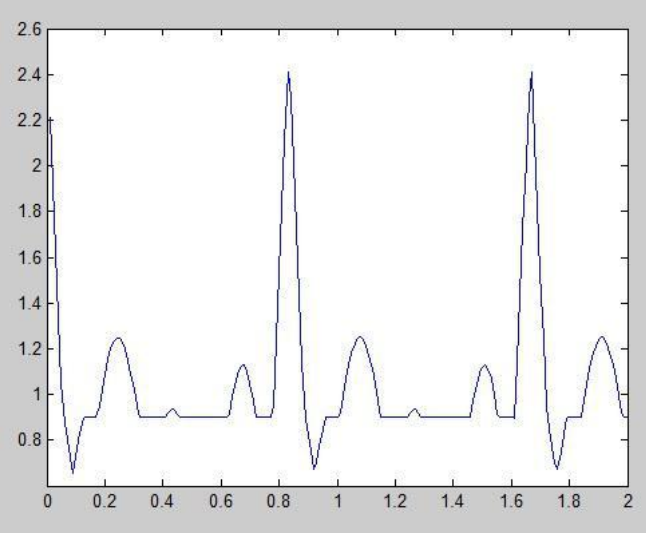

Fig. 4. ECG of healthy person generated using Matlab

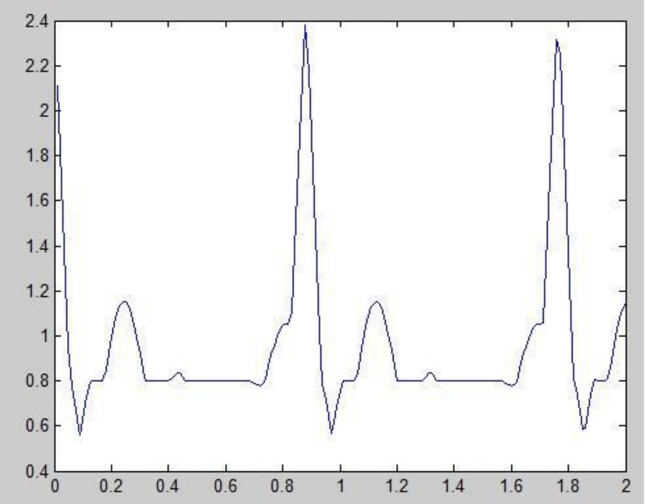

Fig. 5. ECG of person affected Arterial Enlargement; generated using Matlab

VI. CONCLUSION

In the paper a novel MPSoC is proposed. It implements the most popular algorithm and widely adopted by the patient monitoring industry, that is, the Pan and Tompkins QRS detector algorithm, which is based on slope, amplitude and width information. It was developed with Vivado and the Xilinx SDK environment. The implementation parts are operated in parallel and executed concurrently, making possible a real-time and multitask processing.

Based on this successful MPSoC implementation, the future work has for goal to try optimizing, i.e. implementing more software functionalities in such low cost FPGA devices, particularly an algorithm for myocardial ischemia detection.

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