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A Low-Voltage Low-Power Self Biased Bulk-Driven PMOS Cascode Current Mirror

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***Abstract*—A low-voltage low-power self-biased PMOS cascode current mirror employing bulk driven technique is proposed in this paper. The proposed circuit is analyzed and simulated for various parameters including input/output characteristics, output resistance, current linearity, system dc transmission error, power consumption etc. The circuit is implemented using GPDK 180nm CMOS process and is simulated using Cadence Spectre. The simulation results show that: the proposed bulk driven self-bias cascode current mirror has very high current swing, high output impedance, enhanced current linearity and negligible dc transmission error compared to the high output impedance gate driven current mirrors and bulk-driven current mirrors. Further, with the use of PMOS as the active resistance, the power consumption of the circuit is also reduced drastically. Thus the proposed design finds wide acceptability and usability in low voltage low-power CMOS analog integrated circuits.**

Keywords—Low-Voltage, Low-Power, CMOS, self-bias, Current Mirror, high swing, high impedance, bulk-driven.

I. INTRODUCTION

With the increase in demand of portable devices, low power and low-voltage topologies of analog and mixed-signal designs have gained tremendous importance. In order to make the devices more compact, the concept of scaling down of the device geometry is being used. A low power supply voltage is thus needed to ensure reliability with reduction in device dimensions [1]. However, the power supply voltage cannot be scaled down proportionally to the device dimensions. Consequently, alternate architectures such as self-cascode, sub-threshold, bulk-driven and floating gate have been developed to construct high performance analog circuits with low-voltage power supply.

The bulk-driven technique, which uses bulk terminal as signal input, is emerging as a promising technique for achieving enhanced performance in low voltage analog circuits [1]. This technique enhances the circuit performance, and is compatible with the existing MOSFET structure [2]. It also removes the limitations of threshold voltage effectively by controlling weak positive bias between bulk and source of transistors thus reducing the total supply voltage of the circuit. Furthermore, there is no need to modify standard CMOS process [1].

High performance current mirror is one of the essential and fundamental building blocks in analog integrated circuits. Its applications range from, but not limited to, current amplification, biasing, active loading and level shifting. Hence an efficient current mirror design improves the overall performance of the system. As a low voltage supply is needed to ensure reliability with down scaling VLSI circuits, some new structures of current mirror under low voltage low power configuration needs to be developed to meet the requirements of these low voltage analog integrated circuits.

To gain high output current swing, high output resistance, low power consumption and low input/output voltage drop, a new bulk-driven cascode current mirror (BDCCM) is proposed in this paper. The paper is organized as follows. Section II discusses the existing current mirrors and proposed current mirror design. Section III describes the circuit analysis. Section IV presents the simulation results. Section V concludes the signification of the proposed CM on the basis of simulated results.

II. BASIC OPERATION OF THE CIRCUIT

A. INSPIRATION OF WORK

In the last few years, several current mirror designs having different techniques have been proposed. These designs range from gate-driven technology to bulk-driven technology to sub-threshold technology and more. Fig. 1 shows a low-voltage, very high impedance gate-driven current mirror circuit (GDCM) [3]. This circuit gives high output impedance with low voltage operation.

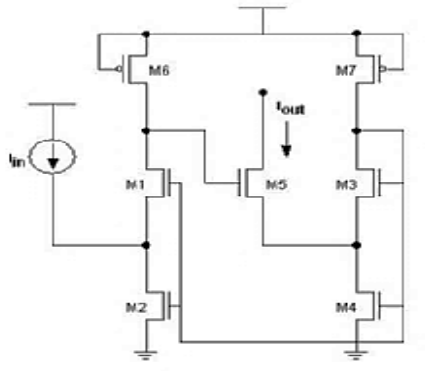


Fig.1 Gate-Driven High Impedance Current mirror

The basic inspirational circuit for this project is low voltage PMOS bulk-driven cascade current mirror circuit (BDCM) [6]. The circuit is shown in Fig. 2.This current mirror has the advantage of low input/output voltage drop and high output swing but it lacks linearity in very low input current range.

B. PROPOSED CURRENT MIRROR

The proposed low-voltage, low-power, self-biased bulk driven current mirror circuit is shown in Fig.3. In this circuit, a constant voltage VG (the lowest potential of the circuits usually) is applied to the gate terminals which creates the inversion layer hence forms the conduction channel beneath the gate. The signals are applied at bulk drain connections unlike at gate-drain connections (as in case of gate-driven current mirrors). Thus, the proposed circuit operates at lower supply voltages as compared to its gate-driven counterparts. In this circuit, as a fixed voltage is given at the gate-terminal and separate voltage at the bulk terminal. The current equation of the MOSFET is modified as the following equation [3]:

$$I_D(sat) = \frac{\beta}{2}(V_{GS} - V_{TH} - \gamma\sqrt{|2\varphi_F - V_{BS}|} + \gamma\sqrt{2\varphi_F})^2$$

$$V_{DS} \le V_{GS} - V_T \text{ ..... (1)}$$

$$\beta = \frac{\mu C_{0X} W}{L}$$

Where , μ is the mobility of the carriers, C_{ox} is the gate oxide capacitance per unit area, W/L is the aspect ratio of the MOSFET, $|\varphi_F|$ is the absolute Fermi potential, VT0 is the zero bias threshold voltage and γ is the body effect coefficient.

In the Eq.(1), in order to have bulk-source junctions reversed biased or slightly forward biased, VBS must be chosen such that it is less than the threshold voltage, hence making bulk currents negligible. The proposed circuit is called self-biased circuit as it does not need a separate biasing source for the bulk of the MOSFETS as the biasing voltage is taken across the PMOS M5 of the circuit itself.

Input signal is directly given to the bulk terminals of M2 and M4, whose source drain currents are built by controlling weak positive bias between bulk and source of transistors. Low-voltage low-power PMOS BDCCM eliminates the limitation of threshold voltage of the signal pathway and hence achieves a low input/output voltage drop.

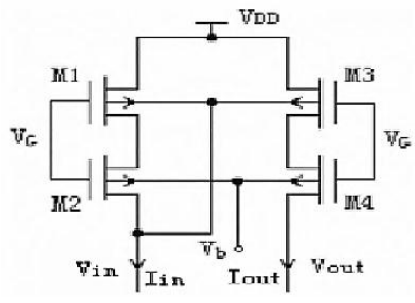


Fig. 2 Low-Voltage PMOS bulk-driven cascade current mirror

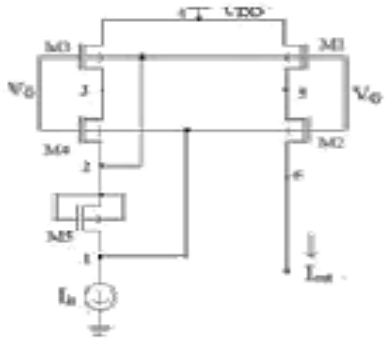


Fig.3 Proposed Bulk-driven Current Mirror

III. CIRCUIT ANALYSIS

Analytical formulations to extract the parameters of the current mirror are performed in the following subsections. Fig. 4 shows the small signal model of the proposed current mirror. In the proposed circuit, M5 is used as an active resistance and therefore represented as a resistance in the small signal analysis.

A. Input/output Voltage characteristics

The minimum input and output voltage drops of low voltage BDCCM may be described as

$$|V_{DD} - V_{IN}|_{(MIN,BD)} = V_{SB3} = V_{SD3} + V_{SD4} + V_{SD5}$$

$$|V_{DD} - V_{OUT}|_{(MIN,BD)} = V_{SD1} + V_{SD2}$$

The minimum input and output voltage drops of high output impedance GDCCM may be described as

$$|V_{DD} - V_{IN}|_{(MIN,BD)} = 2V_{SD,SAT} + |V_T|$$

$$|V_{DD} - V_{OUT}|_{(MIN,BD)} = 2V_{SD,SAT} + |V_T|$$

And here *VSD, sat = VON*

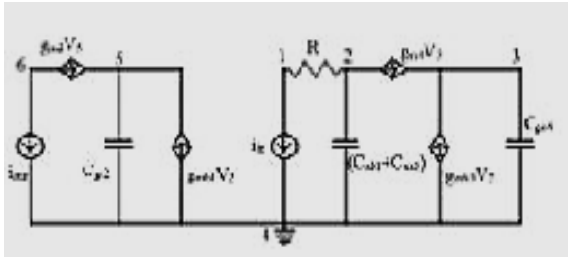


Fig. 4 Small signal model of proposed bulk-driven current mirror

For the weak positive bias between bulk and source of transistor, the input voltage drop of low voltage high output impedance BDCCM is less than or equal to 0.3 V, which is much lower than that of high output impedance GDCCM.

B. DC Transmission Error

The dc transmission error coefficient is defined as

$$\epsilon = (I_{out} - I_{in})/ I_{in}, \text{ (6)}$$

which includes random errors and system errors. Random errors are related to the transistor mismatch parameters and cannot be avoided in the design. It can be reduced only through a good layout design by the centro-symmetric and cross-quading techniques. System errors are related to device structures and are induced by the asymmetric biasing on matched devices. System errors can be reduced

or eliminated through adjusting device parameters. As system errors are the function of device parameters and input current Iin, they are very important for the design of high performance current mirrors. Considering all transistors as matched and random errors as negligible, this paper only deals with system errors.

C. Output Resistance

The output resistance of the proposed circuit is given by the following equation:

$$R_{OUT} = r_{01} + r_{02} + r_{01}r_{02}(g_{m2} + g_{mb2})$$

Thus, above Eq. can be written as:

$$R_{OUT} \approx r_{01}r_{02}(g_{m2} + g_{mb2})$$

where r_{01}, r_{02} are the output resistance of transistors M1 and M2 respectively, g_{m2}, is the transconductance and g_{mb2}, is the bulk transconductance of M2.

D. Power Analysis

The total power consumption of any circuits consists of two components i.e., static and dynamic power consumption. Static power consumption mainly consists of leakage power. As the leakage current is maximum when the biasing voltage of the circuit is minimum, the total power consumed is more at lower voltages. As the biasing voltage increases, conduction channel is formed and hence total power consumption is reduced. The total power consumed by the circuit is measured along with the increasing output voltage (from zero to VDD) to get the power analysis of the circuit over different voltage values.

IV. SIMULATION RESULTS

The circuits shown in this paper including the proposed bulk driven current mirror are simulated using Cadence spectre of 180nm CMOS technology. The design specifications are shown in Table I. The gate driven current mirror shown in Fig.1 operates at 1.8V, the conventional bulk driven current mirror shown in Fig. 2 operates at ±0.8V where as the proposed bulk-driven current mirror operates at ±0.5V, all using the same technology.

Table I. Design Specifications of proposed BDCCM

V_{DD}=0.5V, V_{SS}=-0.5V	
Transistor	**Aspect Ratio, W(µA)/L(µA)**
M1/3	0.4/6
M2/4	0.4/12
M5	2/2

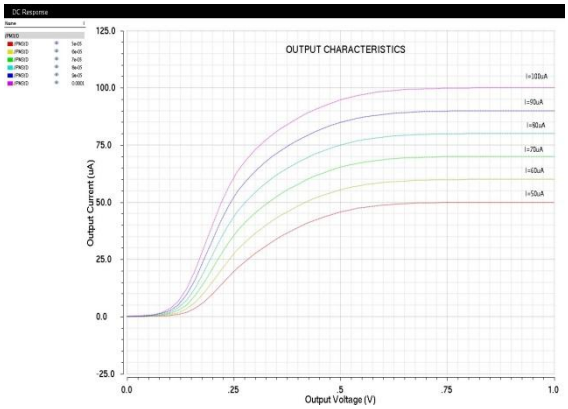


Fig. 5 Iout Vs. Vout of proposed bulk driven current mirror

The output characteristics i.e., output current vs. output voltage is shown in Fig. 5. It can be seen that the circuit starts conducting at a value quite below the threshold value thus reducing the input/output voltage drop of the circuit. Therefore, this circuit is suitable in applications requiring low input voltage and hence reducing the power consumption of the application.

To reflect the high swing operation of the proposed current mirror, Iout vs. Iin graph of the proposed bulk-driven current mirror (proposed BDCCM), gate–driven current mirror (GDCM) and the conventional bulk-driven current mirror (BDCM) are shown in Table2. It can be observed from the graph that the output current shows linearity upto 50uA for GDCM, upto 120uA for BDCM and at least upto 400uA for the proposed BDCCM. Thus the proposed BDCCM is having the maximum current swing.

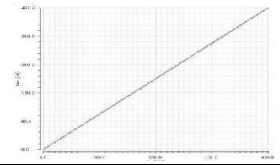
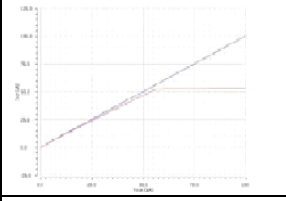
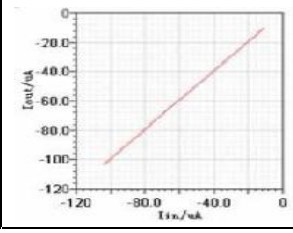
Proposed low-voltage BDCCM	
High Impedance GDCM	
Low-Voltage BDCM	

Table.2 Comparison of different Current mirror
I_{OUT} VS I_{IN}

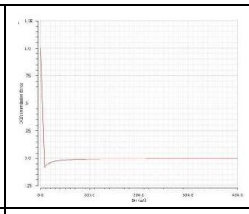
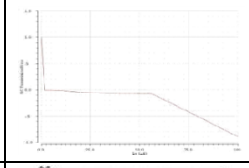
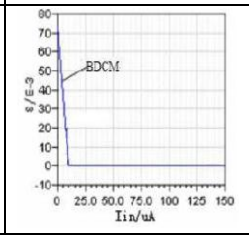
Proposed low-voltage BDCCM	
High Impedance GDCM	
Low-Voltage BDCM	

Table.3 Comparison of different Current mirror
V_{OUT} VS V_{IN}

Table3 Variation curves of Output Current vs. Input Current, shows the DC transmission error graph of proposed BDCCM, GDCM and BDCM respectively. The DC transmission error (ε) is minimum in GDCM for low input current range (<10uA) but as the input current increases, the error starts increasing and becomes very significant as Iin becomes greater than 50uA. Whereas, ε is almost same for BDCM and proposed BDCCM upto 120uA but beyond this range, ε increases significantly for BDCM. This is due to the fact that BDCM is linear upto 120uA whereas proposed BDCCM has very high linearity range of 400uA.

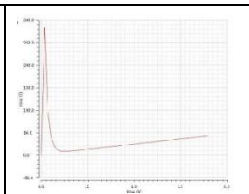
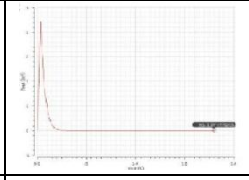
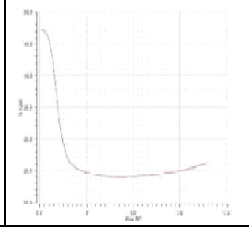
Proposed low-voltage BDCCM	
High Impedance GDCM	
Low-Voltage BDCM	

Table.4 Comparison of different Current mirror

OUTPUT IMPEDANCE VS OUTPUT VOLTAGE

The output resistance of the proposed BDCCM and GDCM is shown in Table.4 for 40uA input current. The input current is so chosen as both the circuits are linear for this input current. As observed from the graph, the output resistance of proposed BDCCM is the same as that of GDCM. Thus the proposed circuit also exhibits very high output impedance. The proposed BDCCM is a very power efficient circuit as it consumes power in µ Watts as compared to mW power consumption in GDCM.

As the leakage current is maximum when the biasing voltage is minimum, the total power consumption is maximum for low biasing voltage. As the voltage increases, the circuit starts conducting, leakage current decreases thus, total power consumption also decreases. The reduced power consumption makes the proposed BDCCM circuit suitable for low power applications.

V. CONCLUSION

The proposed low-voltage, low-power high swing bulk driven current mirror (BDCCM) offers high output current swing, low dc transmission error, high output impedance and low power consumption along with very low input voltage operation. The simulation results show that this design has better performance than its gate-driven and other bulk-driven counterparts. This low voltage, low power bulk-driven design helps to reduce the supply voltage from 1.8V to ±0.5V making it compatible with low power supply requirements of the modern VLSI technology. Thus this design is suitable for wide range of low power, low voltage applications including transmitters, operational amplifiers and source follower etc [8].

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