A Low Voltage Bulk Driven Feed Forward OTA

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Abstract

A low voltage, high swing, pseudo differential Operational Transconductance Amplifier (OTA) is proposed in this paper. This OTA enhances the common mode rejection ratio (CMRR) by using common mode feed forward (CMFF) technique. The design is simulated using Cadence Spectre simulator in 180nm CMOS technology. The OTA can operate at a supply voltage of 0.5V and provides a gain of 49.4 dB, unity gain frequency of 1.3 MHz with output swing of 0.44 V and consumes a power of 3.5µW.

1. Introduction

As the world is advancing to the new heights of development and the need for analog circuits in modern mixed signal VLSI chips for multimedia, control, instrumentation, medical, electronics and communication is increasing, so new technologies are being developed that enable the designers to create faster, complex, portable and energy operated systems within the permissible limit of power consumption. Low power supply analog circuits demand reduction in their supply voltage but the reduction in supply voltage will cause many problems as the threshold voltage ($V_T$) of the analog circuits has been reduced at a slower rate than their supply voltage which causes reduction in the available signal swing. So for reducing the threshold voltage ($V_T$) many techniques have been used [1, 2].

[3, 4] proposed bulk-driven which is used in the input stage proves to be useful alternative for designing the amplifiers able to operate with a low supply voltage which is in the order of threshold voltage. The input voltage applied to bulk and the gate voltage is tied to some bias which reduces the threshold voltage of the transistor. So, the threshold voltage can be removed from the signal path and enabling the circuit to operate at a low supply voltage. The expression for the threshold voltage in bulk driven MOS [5] can be given as in (1)

$$V_T = V_{TO} + \gamma (|2\Phi_F - V_{SB}| + |2\Phi_F|)$$

(1)

where $\gamma$ is the body effect coefficient, $\Phi_F$ is the Fermi potential and $V_{SB}$ is the source to bulk potential. The main drawback of bulk driven technique is the bulk transconductance ($g_{mb}$) is 4 to 5 times smaller than the gate transconductance ($g_m$) which results in low DC gain. Another approach for low power, low voltage design is to utilize subthreshold region for operating the circuit [6].

The Operational Transconductance Amplifier (OTA) is one of the most important and frequently used analog building blocks as OTA finds many applications in many analog circuits such as comparators, ADCs and so on. Several approaches have been proposed for realizing OTA [7-9] using both fully-differential (FD) and pseudo-differential (PD) topologies. The main difference between FD and PD is that PD is typically based on differential pair with a tail current source while PD is based on two independent inverters without tail current source. Advantage of using PD is that it avoids the voltage drop across the tail current source which allows wider input and output ranges and makes circuit attractive for low power applications. However, for suppressing common-mode signal, PD structure requires an extra common-mode feedback (CMFB) circuit, thus degrading the performance as CMFB behaves like an additional load. Furthermore, CMFB circuit has to be carefully designed to avoid stability problems, resulting in complex circuitry and more power consumption. So an alternative is to use common-mode feed forward (CMFF) technique. [10] shows that the CMFF performs better in terms of induced nonlinear, signal distortion, speed and output signal swing and feed-
forward approach results very attractive for low-voltage applications.

In this work, a low voltage pseudo-differential OTA using bulk-driven technique is proposed. The circuit uses a feed forward technique to suppress common mode signals and enhances the differential-mode signals, and operates in the subthreshold region.

2. Proposed pseudo differential OTA

A. Bulk input pseudo differential OTA

A basic low voltage bulk driven PD-OTA is shown in Fig. 1. The circuit consists of two independent bulk input PMOS (M1a,b) and two active load NMOS transistors (M2a,b). The gate voltages for PMOS and NMOS are biased to a constant voltage Vb1 and Vb2 respectively for operating in subthreshold region.

![Fig.1 Bulk input PD-OTA.](http://example.com)

In PD structure, removing the tail current source results in larger common-mode gain (A_CM) where as in FD structure the common-mode gain is increased by increasing the output resistance of the bias current source. However, for PD shown in Fig. 1, the common-mode gain (A_CM) is equal to the differential-gain (A_DM).

The differential-mode gain for the above circuit is given in (2)

\[ A_{DM} = g_{mh1,2} |r_{o2}| \]  

The CMRR calculated for the above circuit is given in (3)

\[ CMRR = \frac{A_{DM}}{A_{CM}} = 1 \]  

which results in unity. This large A_CM in PD structure results in huge common-mode variations at the OTA output.

B. Common mode Feed Forward

The CMRR problem can be solved by using common-mode feed forward technique. Fig. 2 shows the CMFF topology for bulk driven circuit. This method reduces the common-mode signal at the input nodes by feeding them inversely through another path forward to the output nodes. The common-mode signals which come from both the paths would be cancelled at the output node by superposition addition which results in the increase of CMRR while the common-mode gain is decreased.

![Fig.2. Common mode Feed Forward Method](http://example.com)

C. Bulk driven Feed Forward OTA

A bulk driven OTA with common-mode feed forward technique is shown in Fig. 3. The common feed forward circuit concept is taken from [9], but this circuit operates in the subthreshold region. For operating the circuit near moderate inversion or weak inversion side of moderate inversion region, a large voltage can be applied as a gate bias and the signal can be applied to the body of the device in order to attain a relatively large body transconductance. The input is applied to the body of PMOS transistors M1 and M2, and their g_{mb} provides the input transconductance. For an input common-mode voltage of VDD/2 the resulting small body-source forward bias lowers the V_T and further increases the inversion level. The body inputs of M3 and M4 form cross coupled pair that boosts the differential DC gain by adding negative resistance to the output. The current equation for the subthreshold region operating in weak inversion is given by (4)

\[ I_d = \frac{W}{L} \mu \frac{K T}{q} \left[ \frac{q N_{CH} \Phi_F}{4 \Phi_F} \exp \left( \frac{V_{GS}-V_T}{n K T/q} \right) \right] \]  

where \( \Phi_F \) is the Fermi potential, \( N_{CH} \) is the channel doping, \( V_{GS} \) is the gate to source potential, \( K \) is the Boltzmann constant and \( q \) is the electron charge.
bulk driven circuit the current expression is given by
(5)
\[ I_d = \frac{W}{L} \mu (\frac{K T}{q})^2 \sqrt{\frac{q S G N_{ch} \theta}{4 \Phi_F}} \exp\left( \frac{V_{GS} - V_T - \sqrt{2 \Phi_F - V_{BS} + \gamma \sqrt{2 \Phi_F}}}{n K T / q} \right) \]

where \( V_{BS} \) is the bulk to source potential, \( V_T \) is the threshold voltage when bulk-source is at 0V and \( n \) is the subthreshold slope factor.

The bulk transconductance \( g_{mb} \) can be obtained by differentiating (5) with respect to \( V_{BS} \) and is given as in
(6)
\[ g_{mb} = \frac{I_d}{n K T / q \sqrt{2 \Phi_F - V_{BS}}} \]

Fig. 3 Bulk driven Feed Forward OTA

The common-mode signal is strongly suppressed as a result of \( g_{mb2} \) being larger than \( g_{mb1,2} \) and is intrinsically less than 1.

In this design the differential gain \( A_{DM} \) can be increased by cascading two identical gain blocks to form a two-stage OTA as shown in Fig. 4. To increase the stability Miller compensation capacitors \( C_C \) with series resistors \( R_C \) was added to move the right half-plane zero to left half-plane zero. The unity gain-bandwidth product is given by (7) and the second pole frequency is given by (8) as in [3, 4].

\[ GBW = \frac{g_{mb1,2}}{2 \pi C_C} \]  

(7)

\[ GBW = \frac{g_{mb1,2}''}{2 \pi f_L} \]  

(8)

where \( g_{mb1,2} \) and \( g_{mb1,2}'' \) are the input transconductance of the first and the second stage.

4. Simulation results

The designed OTA was simulated with Cadence Spectre simulator using 180nm CMOS technology with threshold voltage less than 0.45V for both PMOS and NMOS to operate under supply voltage. The aspect ratios of all the transistors are shown in Table 1.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>ASPECT RATIOS OF TRANSISTORS</th>
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</thead>
<tbody>
<tr>
<td>FIRST STAGE(PARAMETER)</td>
<td>VALUE</td>
</tr>
<tr>
<td>(W/L)_{1,2}</td>
<td>10.01\mu/180n</td>
</tr>
<tr>
<td>(W/L)_{3,4}</td>
<td>500n/475n</td>
</tr>
<tr>
<td>(W/L)_{5,6}</td>
<td>400n/180n</td>
</tr>
<tr>
<td>(W/L)_{7,8,9,10}</td>
<td>12 \mu/950n</td>
</tr>
<tr>
<td>(W/L)_{11,12,13,14}</td>
<td>9.95 \mu/1.25 \mu</td>
</tr>
<tr>
<td>SECOND STAGE</td>
<td></td>
</tr>
<tr>
<td>(W/L)_{1,2}''</td>
<td>10.01\mu/180n</td>
</tr>
<tr>
<td>(W/L)_{3,4}''</td>
<td>500n/475n</td>
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</tr>
</tbody>
</table>

Fig. 4 Two Stage OTA

The aspect ratios of all the transistors are shown in Table 1.

GBW= \[ \frac{g_{mb1,2}}{2 \pi C_C} \]  

(7)

GBW= \[ \frac{g_{mb1,2}''}{2 \pi f_L} \]  

(8)
The common-mode signal is suppressed using Feed Forward technique as the common mode gain is found to be -182.4 dB which is obtained by applying a common mode input signal of 10mV and shown as in Fig.7. The CMRR is obtained above 200 dB which is calculated by (9).

\[
CMRR = \frac{A_{DM}}{A_{CM}}(9)
\]

The simulation results are summarised in Table 2.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
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</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>0.5V</td>
</tr>
<tr>
<td>Gain</td>
<td>49.4dB</td>
</tr>
<tr>
<td>Unity Gain frequency</td>
<td>1.3MHz</td>
</tr>
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</table>
5. Conclusion

In this paper, a bulk driven CMOS pseudo differential OTA is proposed. The design incorporates the feed forward technique which suppresses the common mode gain and gives a differential gain of 49.4 dB with unity gain frequency of 1.3 MHz for a phase margin of 22.6°. The circuit gives high output swing with a power dissipation of 3.5\( \mu \)W.

6. References


