A Low Phase Noise Wide Tuning Range CMOS Differential Ring Voltage Controlled Oscillator for Signal Processing

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***Abstract*- This paper presents a detailed two stage ring oscillator in CMOS standard 45nm technology. This VCO operates in the range of 2.5 GHz to 7.7 GHz. Along with that low phase noise and low power consumption is estimated in this circuit. It operates at very low voltage of 1V and hence can be used in low power receiver circuits in signal processing applications.**

Keywords:- PLL, Cadence, offset, Ring VCO

I. INTRODUCTION

The growing downscaling and miniaturization of electronic circuits to embed multi-tasking features into a complete system motivates the researchers to work on various circuits. In latter-day practical application, Integration industries are dealing with Portable structures. To amend the circuit simulation time and to obtain high performance of the device, the representation is chosen to develop VCO using CMOS technology. To meet the clock generation systems in electronic devices Voltage Control Oscillator and Current Control Oscillators are very widely used in wireless communication systems, include phase lock loop, clock data recovery etc. To meet the essentials of portability, electronic systems are necessarily made to use low-voltage, high signal to noise ratio (SNR). Therefore, to achieve an effective design with less voltage full-swing on chip VCO is requisite.

The major concern of VCO design is variation in the output phase and frequency synthesis for which result in amplitude noise. Achieving high frequency results in higher VCO gain and degradation in performance with other parameters. In addition, non-linear VCO characteristics degrades PLL stability the noise in the output frequency is proportional to the VCO gain. In common wide range VCOs, the wide frequency range is covered using multiple ring oscillators, each working in different frequency ranges. In [1], the authors propose a CMOS VCO for PLL application with wide frequency range using multi ring oscillator with different frequencies. For frequency variation external trim bits are used. In [2], a ring voltage control oscillator posses' low power with wide tuning range and differential stages are designed to reduce phase noise.

II. CIRCUIT ANALYSIS: A REVIEW

From the literature review it has been verified that different frequency operating range of VCO have implemented with various topologies using ring VCO. Basically, CMOS based VCO can be designed using two ways, firstly LC-VCO and secondly ring VCO [3]. Ring VCOs are more preferred as it can be operated in higher frequency ranges and can be designed in very less design space. A part from the topological variations other CMOS techniques are performed on VCO to design and exhibit frequency of 87-910 MHz with tuning voltage of 0.7-2.3V [4]. As single stage circuit has low phase noise due to reduced noise source. And operate with the oscillation frequency 5.6 GHz and power consumption of 4.8mW at same operating frequency [5]. The design of VCO is developed using current control oscillator and schmitt trigger by using voltage to current converter and obtain frequency range of 68-258MHz. [6] the approach of voltage-controlled ring oscillator based on the voltage controlled switch is proposed in 0.13m CMOS technology with supply voltage of 3.3 V. A VCO with high frequency range from 2.26 GHz to 3.50 GHz. [7] representing the nine stages of differential delay cells with multiple pass loop architecture and estimating wide tuning range is shown in [8]. The designed circuit topology constructed in a modified conventional current reused configuration. It is adopt two dc level shifters and using negative resistance enhancement technique [9] the linearity of the oscillator is improved by applying a feedback loop using a switched-capacitor network as a frequency-to-voltage converter (FVC) [10]. A fully switching differential delay cell is employed to reduce the phase noise of the ring oscillator. It utilizes dual-delay path techniques to achieve high oscillation frequency and obtain a wide tuning range.
The ring VCO [11] proposed in this paper uses a novel single ended delay cell and is designed to achieve the requirement of a low-supply voltage, low power consumption, low phase noise.

III. PROPOSED CIRCUIT

The schematic circuit of the delay cell is shown in Figure-1. From the figure it can be shown that it uses differential pair of PMOS (PM3 & PM4). This pair is connected in positive feedback pattern. This helps to

reduce the delay and hence increase the speed of operation of the oscillator. Also it helps in reducing the jitter of the oscillator. The negative feedback circuit can induce more stability and improvisation in speed of the circuits but the resistivity of the circuit increases and hence power consumption may increase. The oscillator frequency of operation is basically controlled by the controlled voltage which is connected to the two PMOS (PM1 & PM2). There are two transconductance NMOS (NM1 & NM2) which increases the ratio between transconductance to capacitance and hence enhances the frequency of operation. The use of this type of configurations reduces the use of current mirror circuit and as a result of which the area of the circuit can be minimized.

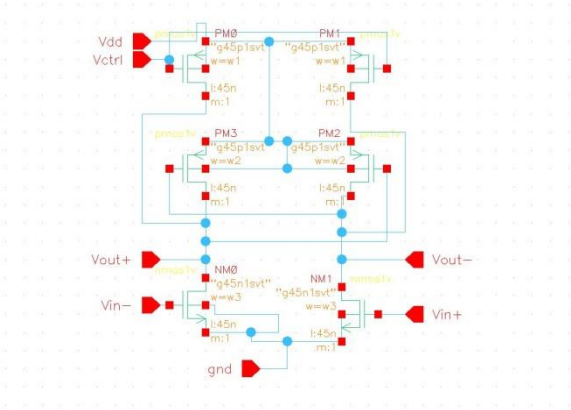

Figure.1: A delay Cell

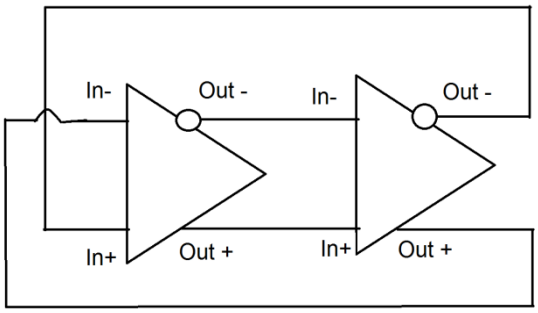

Figure.2: Two stage implementation of delay cell

III. SIMULATION RESULTS

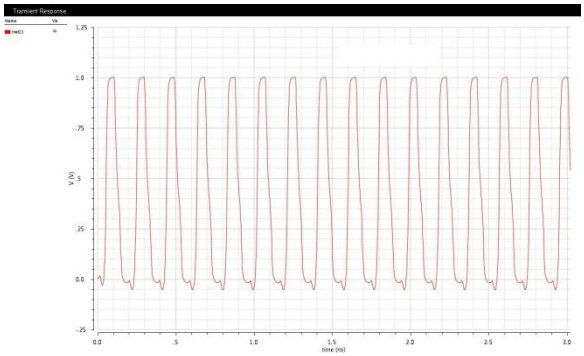

Figure.3: Frequency Analysis

The above two stage VCO is designed and implemented in Cadence Virtuoso in gpdk 45nm CMOS technology. The various parameters are extracted and found out using Cadence Spectre tool. In figure 3, the transient analysis of VCO shows the frequency of operation at 5.176 GHz at 1 V input supply.

Figure 4 shows the static power consumption which is as low as 2.188 uW. Similarly, the phase noise calculated to be -96.148 dBc/Hz at 1 MHz offset when tuned properly i.e. the sizing of the transistors done. Subsequently, layout of the circuit is designed for the circuit having no DRC and LVS error and its area calculated to be of 3.5 x 4.05 um x um which is shown in figure 6.

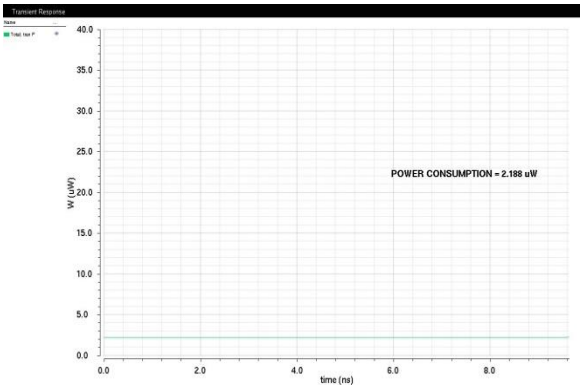

Figure.4: Static Power Consumption

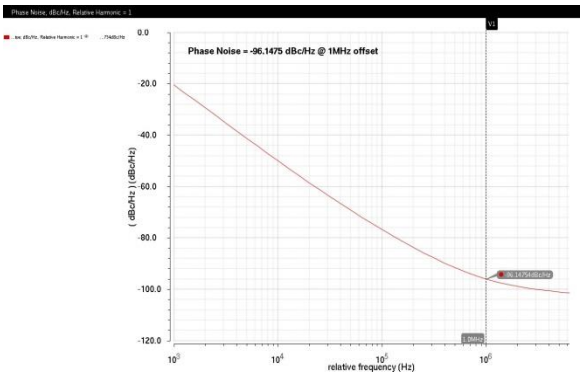

Figure.5: Phase noise at 1 MHz offset

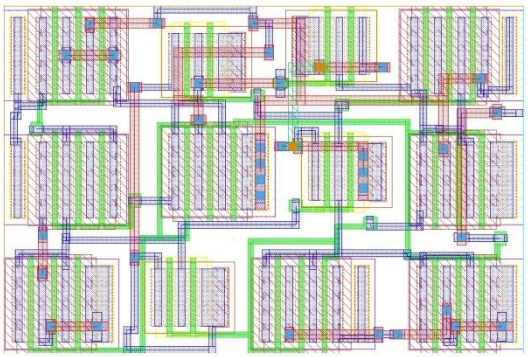

Figure.6: Layout of the circuit

Table-1: Corner Analysis of the circuit of various design parameters

Design Parameters	Typical	FF	FS	SF	SS
Frequency (in MHz)	10.67	48.24	32.23	5.11	1.76
Power (in uW)	18.90	42.52	19.30	18.56	7.34
Phase Noise (in dBc/Hz) @ 1MHz offset	-96.15	-85.43	-86.76	-95.93	Failed

Table-2: Analysis of various parameters in varied temperature

Design Parameters/	Temperature		
	-25 ºC	50 ºC	125 ºC
Frequency (in MHz)	4.64	14.26	29.89
Power (in uW)	13.88	20.55	23.56

The circuit is analyzed in-depth manner are and simulated at various testing conditions. In table-1, it shows the corner analysis in 5 different states. In table-2, it shows the operation capability of the VCO from -25ºC to 125ºC. From the table it can be inferred that the circuit can be operated in various tricky conditions as well and variation affected is very less. In table-3, a comparison has been made with the VCO simulated in this paper and some other research papers. The VCO operating in this technology has very low phase noise but compromising the operating frequency.

Table 3: Comparative results of various VCO

Design Parameters	[12]	[10]	[14]	[15]	[3]	This Work
Process Technology (in nm)	500	180	130	90	45	45
Supply Voltage	2.5	2.0	1.6	1.5	1	1
Frequency Range (in MHz)	660-1270	737-1456	1GHz-9GHz	1220-3220	6 GHz-17 GHz	2-50
Power	15.50 mW	14.80 mW	6.0 mW	9.61 mW	2.97 uW	18.90 uW
Phase Noise (in dBc/Hz)	-106 @ 0.6 MHz	-103 @ 0.6 MHz	-106 @ 10MHz	-90 @ 600 kHz	-78 @ 10 MHz	-96.2 @ 1 MHz

CONCLUSION

A very low phase noise based voltage controlled oscillator has been proposed in this paper. From the simulation results and comparison with other papers it has been found that it can operate at a wide range of frequency with less power consumption of 18.90 uW due to less supplied voltage of 1 V. Phase noise which is -96.475 dBc/Hz @ 1 MHz offset which is better for ring oscillator. From the corner analysis, it can be stated that there is very less variation in various parameters calculated from the simulation results. So, this circuit if implemented can be fruitful in various communication blocks in harse conditions. Although the operating frequency has been compromised but still various signal processing applications can be implemented using this oscillator.

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