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A High Voltage Gain Interleaved Boost Converter with Dual Coupled Inductors

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***Abstract*— A high gain interleaved boost converter with dual coupled-inductors and a voltage multiplier module is proposed. The primary windings of two coupled-inductors are connected in parallel to share the input current and reduce the current ripple at the input. The proposed converter inherits the merits of interleaved series-connected output capacitors for high voltage gain, low output voltage ripple and low switch voltage stress. Moreover, the secondary sides of two coupled-inductors are connected in series to a regenerative capacitor by a diode for extending the voltage gain and balancing the primary-parallel currents. In addition, the active switches are turned on at zero-current and the reverse recovery problem of diodes is alleviated by reasonable leakage inductances of the coupled inductors. Besides, the energy of leakage inductances can be recycled.**

Keywords*— Renewable energy, photovoltaic system, interleaved boost converter, dual coupled inductors,high voltage gain.

I. INTRODUCTION

Renewable energy attracts interest for power generation because the non renewable energy like petrol, diesels etc are diminishing and energy crisis is an important concern in most of the nations. In renewable energy, solar energy attracts more because it has more advantage compare to other renewable energies like the selection of area is not complicated, the systems can either be operated as isolated systems or connected to the grid as a part of an integrated system, it has no moving parts; it has a long lifetime and low maintenance requirements and most importantly it is one solution that offers eco friendly power [4]. Photovoltaic system requires a power electronics interface to be connected to the grid. Renewable energy systems generate low voltage output. So high voltage gain DC-DC converters are required in many industrial applications.

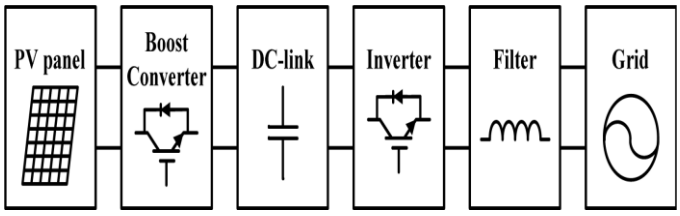

Fig.1. Photovoltaic system

Photovoltaic (PV) energy conversion systems and fuel-cell systems usually need high step-up and large input current dc-dc converters to boost low voltage (18–56V) to high voltage (200–400V) for the grid-connected inverters. High-intensity discharge lamp ballasts for automobile headlamps call for high voltage gain dc-dc converters to raise a battery voltage of 12V up to 100V at steady operation [5], [6]. Also, the low battery voltage of 48V needs to be converted to 380V in the front-end stage in some uninterruptible power supplies (UPS) and telecommunication systems by high step-up converters [7]-[8]. Theoretically, a basic boost converter can provide infinite voltage gain with extremely high duty ratio. In practice, the voltage gain is limited by the parasitic elements of the power devices, inductor and capacitor. Moreover, the extremely high duty cycle operation may induce serious reverse-recovery problem of the rectifier diode and large current ripples which increase the conduction losses. On the other hand, the input current is usually large in high output voltage and high power conversion, but low-voltage-rated power devices with small on-resistances may not be selected since the voltage stress of the main switch and diode is respectively equivalent to the output voltage in the conventional boost converter.

The interleaving technique connects dc/dc converters in parallel to share the power flow between two or more conversion chains. However, the conventional interleaved converter has some disadvantages like the duty ratio is extremely large in order to get a high gain, this increases the current ripple, conduction losses and the turnoff losses. Then, the switches voltage stress is the high and the output diode reverse-recovery problem is very severe, which induces additional voltage and current stresses and losses and also the electromagnetic interference (EMI) noise is very serious[9]. Single switch topologies are not suitable for high power applications because voltage stress across switch is very high. Interleaved parallel topology is the solution to increase the power and reduce input current ripple allowing lower power rated switches to be used. This paper proposes a high voltage gain interleaved boost converter with dual coupled inductors for high step up and high power applications. This configuration inherits the merits of high voltage gain, low output voltage ripple and low-voltage stress across the power switches. Moreover, the presented converter is able to turn on the active switches at zero-current and alleviate the reverse recovery problem of diodes by reasonable leakage inductances of the coupled inductors.

II. PROPOSED SYSTEM

A high voltage gain interleaved boost converter with dual coupled inductors for high step up and high power

applications is proposed. The derivation procedure for the proposed topology is shown in Fig. 2. This circuit can be divided as two parts. These two segments are named a modified interleaved boost converter and a voltage doubler module using capacitor-diode and coupled inductor technologies. The basic boost converter topology is shown in Fig. 2(a) and Fig .2(b) is another boost version with the same function in which the output diode is placed on the negative dc-link rail. Fig.2(c) is called a modified interleaved boost converter, which is an input-parallel and output-series configuration derived from two basic boost types.

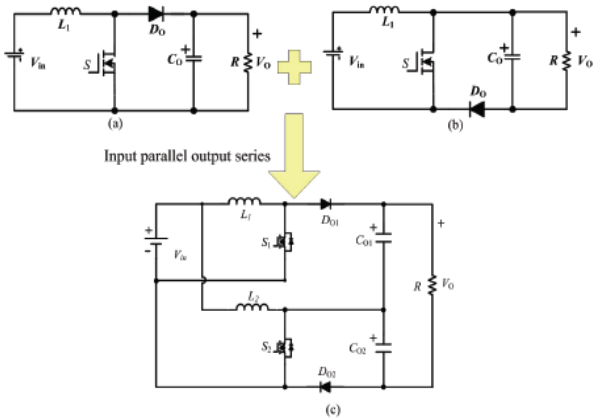

Fig.2. Modified interleaved boost converter

Therefore, this part based on interleaved control has several main functions: 1) it can obtain double voltage gain of conventional interleaved boost; 2) low output voltage ripple due to the interleaved series-connected capacitors; 3) low switch voltage stresses. Then the double independent inductors in the modified interleaved boost converter are separately replaced by the primary windings of coupled inductors which are employed as energy storage and filtering as shown in Fig.3 (d). The secondary windings of two coupled inductors are connected in series for a voltage multiplier module, which is stacked on the output of the modified converter to get higher voltage gain.

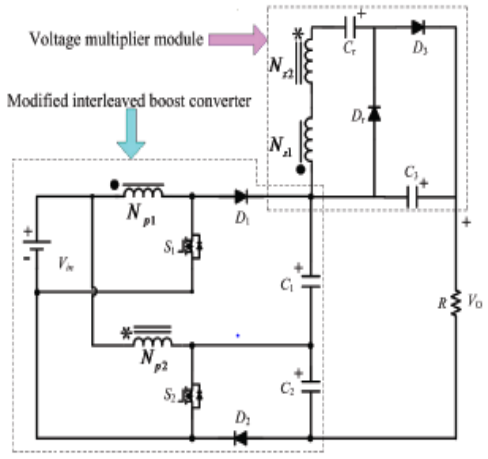

Fig.3. Interleaved boost converter with dual coupled inductors

Advantages of the proposed converter are

1) It can achieve a much higher voltage gain and avoid operating at extreme duty cycle and numerous turn ratios
2) The voltage stresses of the main switches are very low, which are one fourth of the output voltage under N=1
3) The input current can be automatically shared by each phase and low ripple currents are obtained at input
4) The main switches can be turned on at ZCS so that the main switching losses are reduced;
5) The current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated

III. OPERATION PRINCIPLE

The proposed converter operates in continuous conduction mode (CCM), and the duty cycles of the power switches during steady operation are interleaved with a 180◦ phase shift and the duty cycles are greater than 0.5. That is to say, the two switches can only be in one of three states (S1:on, S2:on; S1:on,S2:off; S1:off,S2:on;), which ensures the normal transmission of energy from the coupled inductor's primary side to the secondary side. The working principle of converter can be explained with eight operating stages. The equivalent circuit of the presented converter is demonstrated in Fig 2, where

L_{m1}, L_{m2}	magnetizing inductances
L_{k1}, L_{k2}	leakage inductances
C_1, C_2, C_3	output and clamp capacitors
S_1, S_2	main switches
D_1, D_2	clamp diodes
D_r, C_r	regenerative diode and capacitor
D_3	output diode
N	turns ratio of N_s /N
V_{N1}, V_{N2}	the voltage on the primary sides of coupled inductors

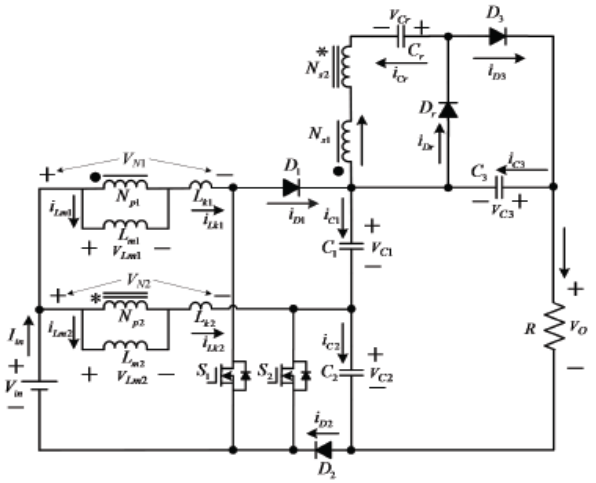

Fig.4. Equivalent circuit

1) First stage [t_0-t_1]: At t = t_0, the power switch S_1 is turned on with zero current switching (ZCS) due to the leakage inductance L_{k1}, while S_2 remains turned on. Diodes D_1, D_2 and D_r are turned off, and only output diode D_3 is conducting. The

current falling rate through the output diode D_3 is controlled by the leak-age inductances L_{k1} and L_{k2}, which alleviates the diodes' reverse recovery problem. This stage ends when the current through the diode D_3 decreases to zero.

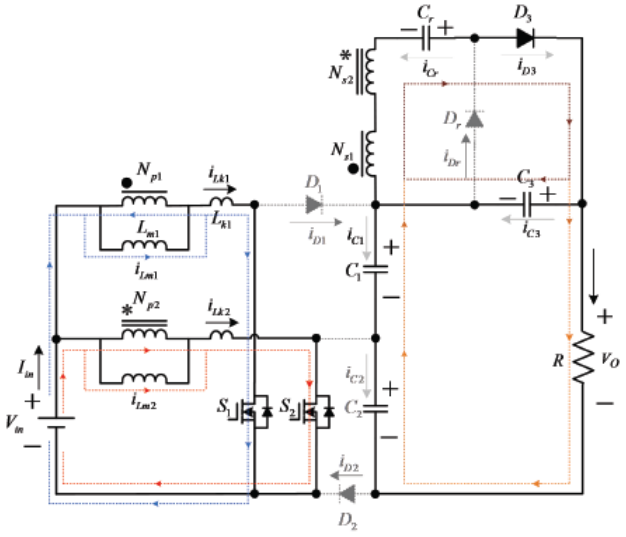

Fig.5. First stage

2) Second stage [t_1-t_2]: During this interval, both the power switches S_1 and S_2 are maintained turned on, as shown in Fig 6. All of the diodes are reversed-biased. The magnetizing inductances L_{m1} and L_{m2} as well as leakage inductances L_{k1} and L_{k2} are linearly charged by the input voltage source V_{in}. This period ends at the instant t_2, when the switch S_2 is turned off.

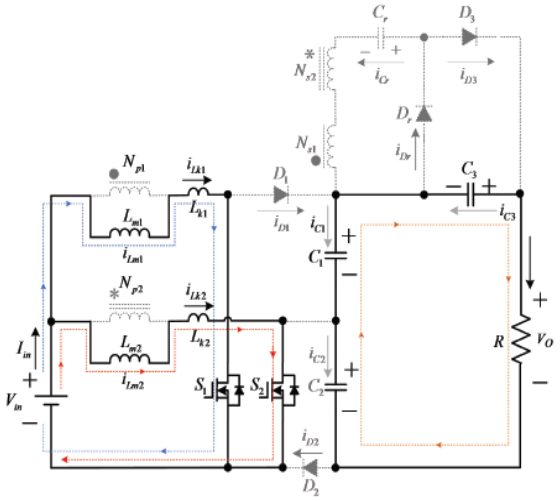

Fig.6. Second stage

3) Third stage [t_2-t_3]: At $t = t_2$, the switch S_2 is turned off, which makes the diodes D_2 and D_r turned on. The current flow path is shown in Fig 7. The energy that magnetizing inductance L_{m2} has stored is transferred to the secondary side charging the capacitor C_r by the diode D_r, and the current through the diode D_r and the capacitor C_r is determined by the leakage inductances L_{k1} and L_{k2}. The input voltage source, magnetizing inductance Lm2 and leakage inductance L_{k2} release energy to the capacitor C_2 via diode D_2.

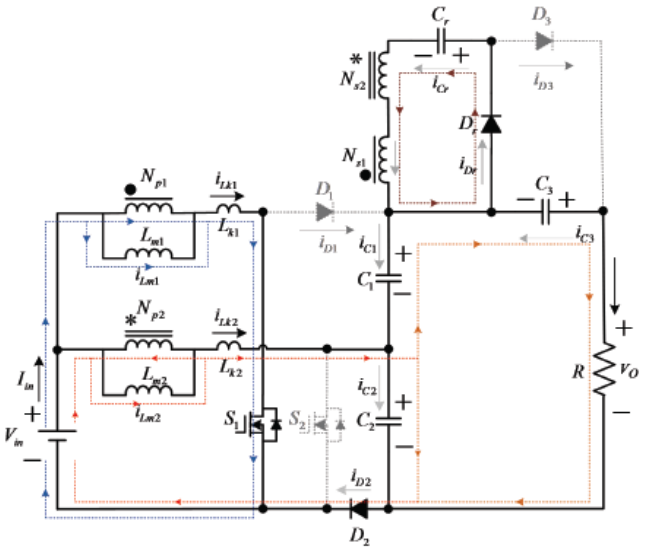

Fig.7. Third stage

4) Fourth stage [t_3-t_4]: At $t = t_3$, diode D_2 automatically switches off because the total energy of leakage inductance L_{k2} has been completely released to the capacitor C_2. There is no reverse recovery problem for the diode D_2. The current-flow path of this stage is shown in Fig 8. Magnetizing inductance L_{m2} still transfers energy to the secondary side charging the capacitor C_r via diode D_r. The current of the switch S_1 is equal to the summation of the currents of the magnetizing inductances L_{m1} and L_{m2}.

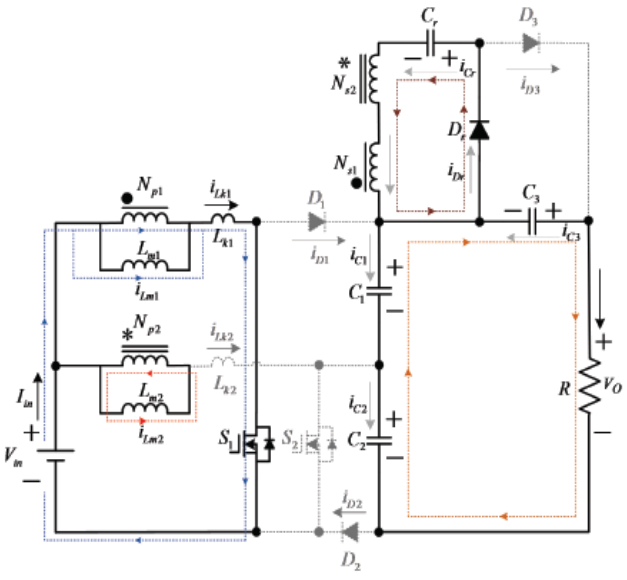

Fig.8. Fourth stage

5) Fifth stage [t_4-t_5]: At $t = t_4$, the switch S_2 is turned on with ZCS soft-switching condition Due to the leakage inductance L_{k2}, and the switch S_1 remains in on state. The current-flow path of this stage is shown in Fig 9. The current falling rate through the diode D_r is controlled by the leakage inductances L_{k1} and L_{k2}, which alleviates the diode reverse recovery problem. This stage ends when the current through the diode D_r decreases to zero at $t = t_5$.

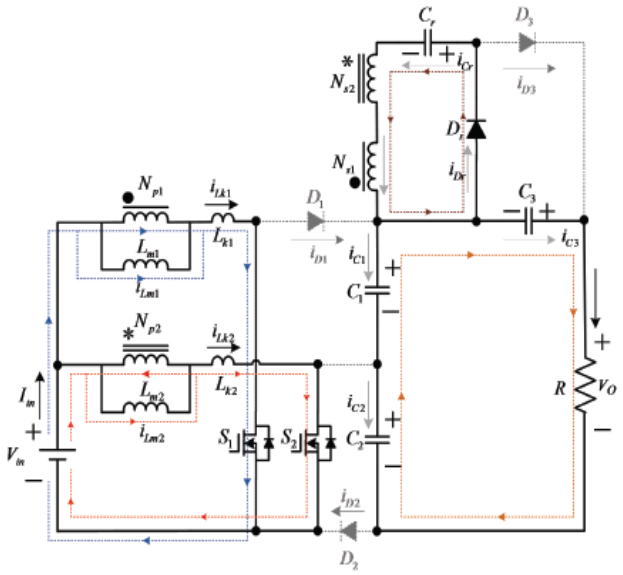

Fig.9. Fifth stage

6) Sixth stage [t_5-t_6]: The operating states of stages 6 and 2 are similar. During this interval, all diodes are turned off. The magnetizing inductances L_{m1}, L_{m2}, and the leakage inductances L_{k1}, L_{k2} are charged linearly by the input voltage. The voltage stress of D_1 is the voltage on C_1, and the voltage stress of D_2 is the voltage on C_2. The voltage stress of D_r is equivalent to the voltage on C_r, and the voltage stress of D_3 is the output voltage minus the voltages on C_1 and C_2 and C_r.

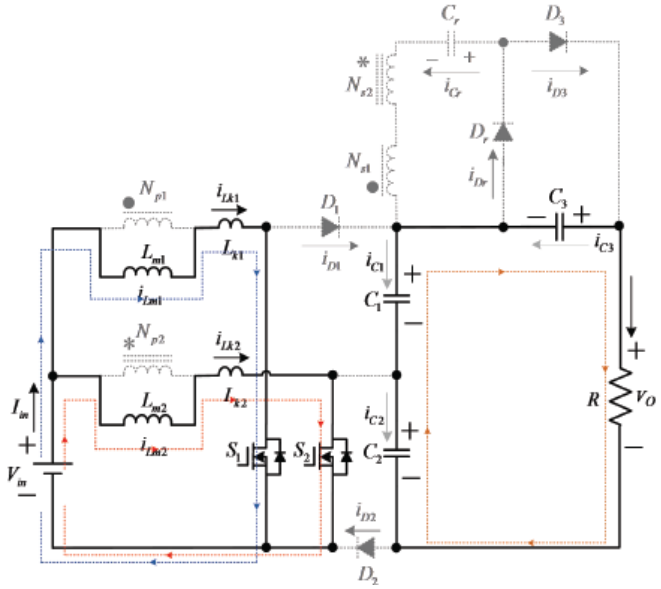

Fig.10. Sixth stage

7) Seventh stage [t_6-t_7]: The power switch S_1 is turned off at $t = t_6$, which turns on D_1 and D_3, and the switch S_2 remains in conducting state. The current-flow path of this stage is shown in Fig10. The input voltage source V_{in}, magnetizing inductance L_{m1} and leakage inductance L_{k1} release their energy to the capacitor C_1 via the switch S_2. Simultaneously, the energy stored in magnetizing inductor L_{m1} is transferred to the secondary side. The current through the secondary sides in series flows to the capacitor C_3 and load through the diode D_3.

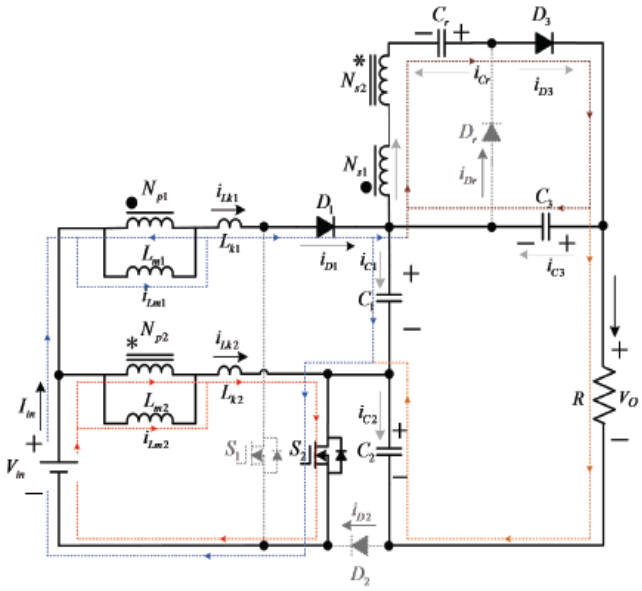

Fig.11. Seventh stage

8) Eighth stage [t_7-t_0]: At $t = t_7$, since the total energy of leakage inductance L_{k1} has been completely released to the capacitor C_1, diode D_1 automatically switches off. The current of the magnetizing inductance L_{m1} is directly transferred to the output through the secondary side of coupled inductor and D_4 until t_0

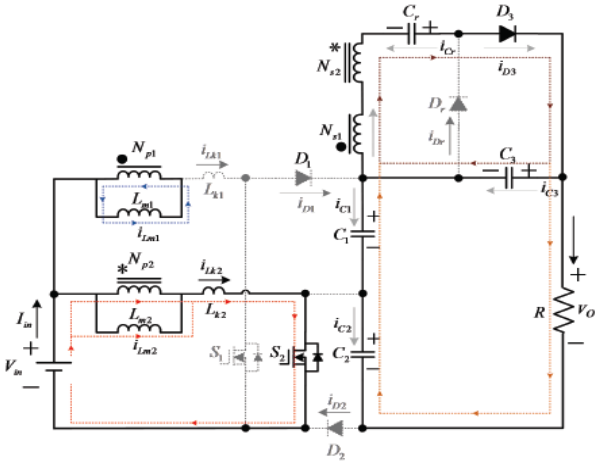

Fig.12. Eighth stage

IV STEADY STATE ANALYSIS

To simplify the circuit performance analysis of the proposed converter in CCM, and the following conditions are assumed.

1) All of the power devices are ideal. That is to say, the on-state resistance $R_{DS}(ON)$ and all parasitic capacitors of the main switches are neglected, and the forward voltage drop of the diodes is ignored;

2) The coupling coefficient k of each coupled-inductor is defined as $L_m/(L_m+L_k)$. The turn ratio N of each coupled-inductor is equal to N_S/N_P;

3) The parameters of two coupled-inductors are considered to be the same, namely $L_{m1} = L_{m2} = L_m$; $L_{k1} = L_{k2} = L_k$; $N_{S1}/N_{P1} = N_{S2}/N_{P2} = N$;
$k_1 = L_{m1}/(L_{m1}+L_{k1}) = k_2 = L_{m2}/(L_{m2}+L_{k2}) = k$.
4) Capacitors $C1$, $C2$, $C3$ and Cr are large enough. Thus, the voltages across these capacitors are considered as constant in one switching period.

A. Voltage Gain Expression

If the transient characteristics of circuit are disregarded, each magnetizing inductance has two main states in one switching period. In one state, the magnetizing inductance is charged by the input source. In the other state, the magnetizing inductance is discharged by the output capacitor voltage V_{C1} or V_{C2} minus the input voltage. Since the time durations of stages I, IV, V and VIII are significantly short, only stages II, III, VI and VII are considered for the steady-state analysis. At stages II and VI, the following equations can be written from Fig.6 and Fig.10.

$$V_{Lm1}^{II} = V_{Lm1}^{IV} = kV_{in} \quad (1)$$

$$V_{Lm2}^{II} = V_{Lm2}^{IV} = kV_{in} \quad (2)$$

$$V_O = V_{C1} + V_{C2} + V_{C3} \quad (3)$$

At stage III, the following equations are derived from Fig. 7:

$$V_{Lm1}^{III} = kV_{in} \quad (4)$$

$$V_{Lm2}^{III} = k(V_{in} - V_{C2}) \quad (5)$$

$$V_{Cr} = V_{S1} - V_{S2} = kNV_{C2} \quad (6)$$

During the time duration of stage VII, the following voltage equations can be expressed based on Fig. 11.

$$V_{Lm1}^{VII} = k(V_{in} - V_{C1}) \quad (7)$$

$$V_{Lm2}^{VII} = kV_{in} \quad (8)$$

$$V_{C3} = V_{Cr} + V_{S2} - V_{S1} = kN(V_{C1} + V_{C2}) \quad (9)$$

Using the volt second balance theory on L_{m1} and L_{m2} respectively the voltage across capacitors $C1$ and $C2$ are obtained as

$$V_{C1} = V_{C2} = \frac{Vin}{1-D} \quad (10)$$

And voltage of capacitors C_r and C_3 are expressed as

$$V_{Cr} = \frac{KN}{1-D} V_{in} \quad (11)$$

$$V_{C3} = \frac{2KN}{1-D} Vi_n \quad (12)$$

Substituting (10) and (12) into (3), the voltage gain is obtained as

$$M_{CCM} = \frac{V_0}{V_{in}} = \frac{2(KN+1)}{1-D} \quad (17)$$

Thus, the plot of the voltage gain M_{CCM} versus the duty-cycle under various coupling coefficients and turns ratio of the coupled-inductor is shown in Fig. 13. It can be seen the coupling coefficient k has only minor influence on the voltage gain. If the impact of the leakage inductances of the coupled inductor is neglected, then coupling coefficient k is equal to one. The ideal voltage gain is rewritten as

$$M_{CCM} = \frac{V_0}{V_{in}} = \frac{2(N+1)}{1-D} \quad (18)$$

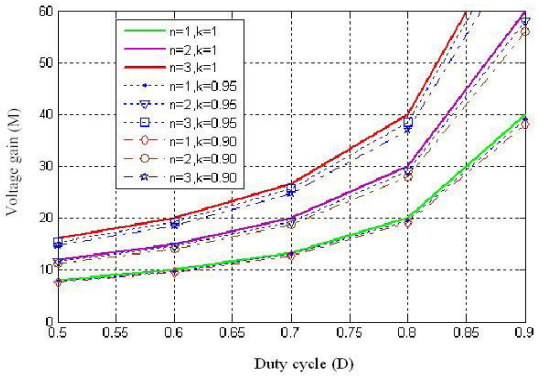

Fig.13. Voltage gain curves under different coupling coefficients

V SIMULATION RESULTS

The simulation is done on MATLAB simulink. The output of the PV system is connected to the boost converter. The simulation diagram of the system is shown in the fig.14.

A Simulation of proposed system

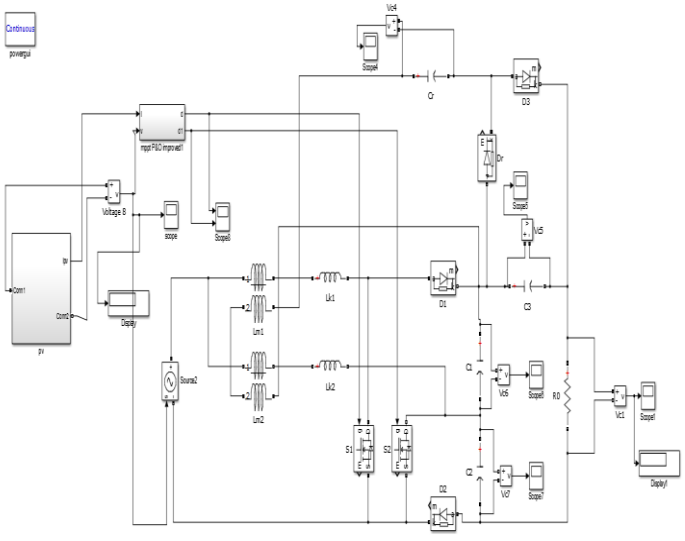

Fig.14. Simulink model of proposed system

B Simulation of PV panel

The PV array has been designed by considering the irradiance, temperature, number of PV cells connected in series and parallel. The simulink model of PV module model is shown in Fig 15. The subsystems (subsystem1 and subsystem 2) for the PV panel modelling are shown in Fig 16 and fig 17

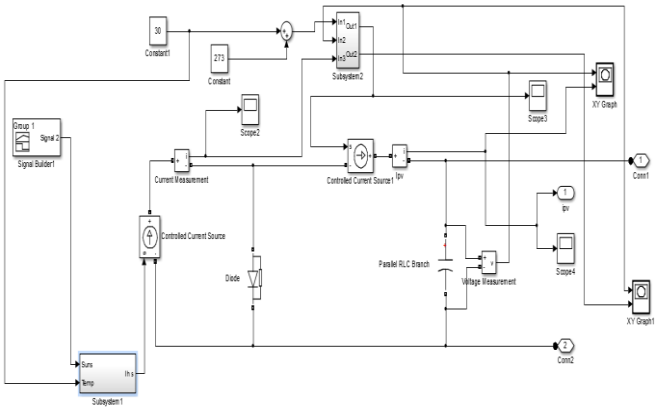

Fig.15. Simulink model of PV panel

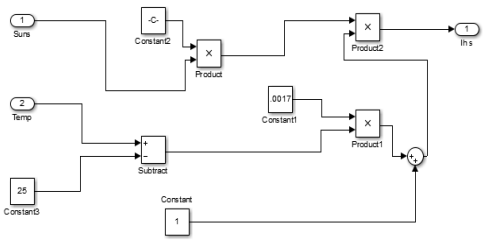

Fig.16. Subsystem 1 of PV panel modelling

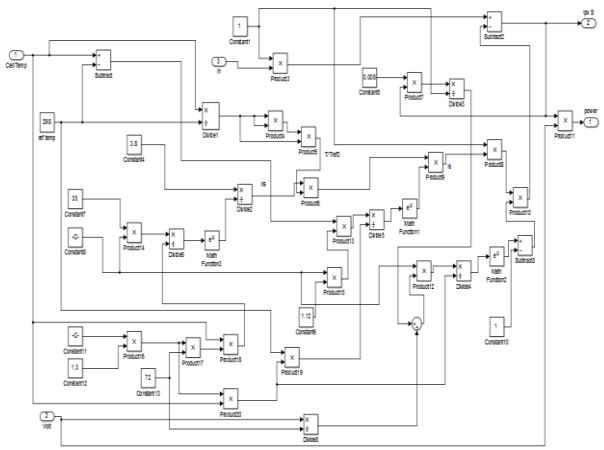

Fig.17. Subsystem 2 of PV panel modelling,

The P-V characteristics and I-V characteristics are shown in the Fig 18 and Fig 19. The PV model plots the P-V and I-V curve for varying values of irradiance. The solar radiation for the system is given by step increment in radiation. The change in radiation is shown in Fig 20.

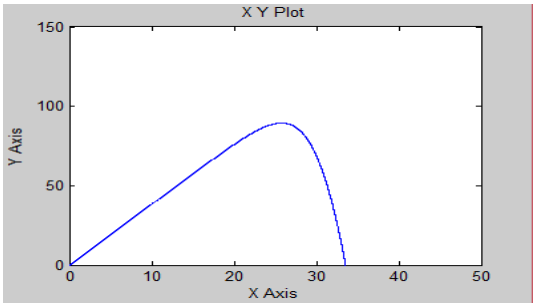

Fig.18. PV characteristics

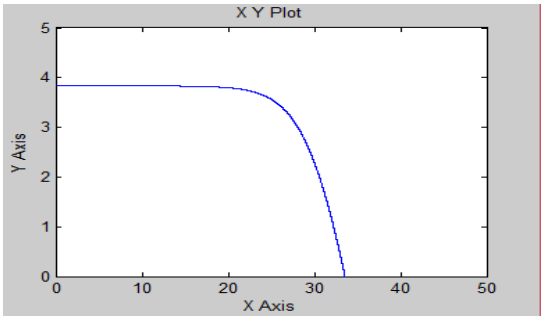

Fig.19. IV characteristics

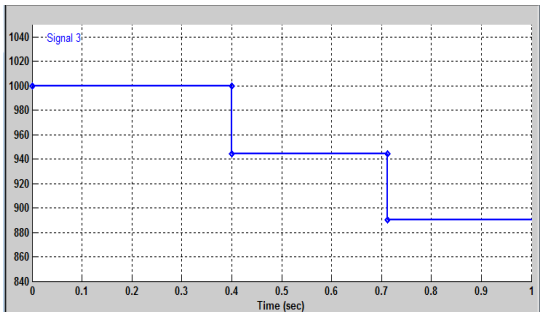

Fig.20. Change in irradianc

C Simulation of MPPT Technique

The MPPT technique is simulated with the principle of P & O algorithm. The signal obtained from the algorithm is given to the gate of boost converter for the operation. The simulation model of the MPPT algorithm is shown in Fig 21.

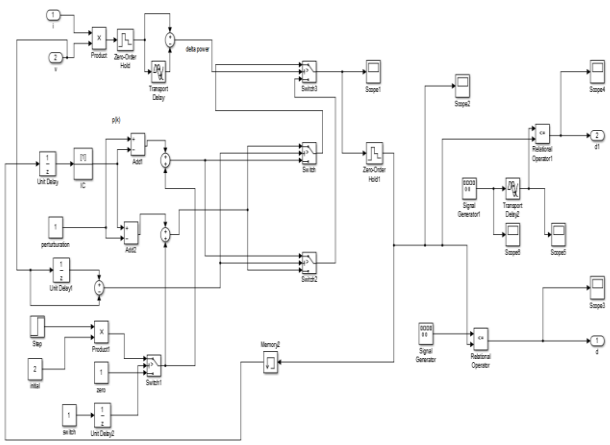

Fig.21. Simulink model of MPPT

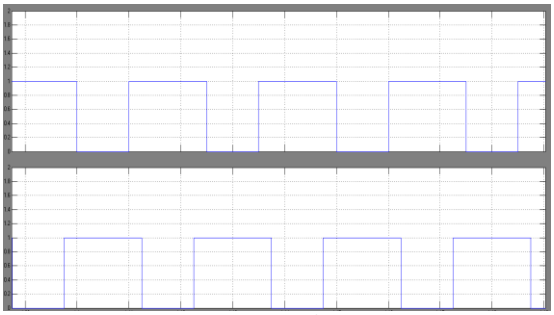

Fig.22. Gate pulses from MPPT

D Simulation results of interleaved boost converter

The converter works in continuous mode of operation, with a phase shift of 180° and duty cycle greater than 0.5. The output voltage across the converter for an input of 38V from PV system is 380V. So the gain is 10 for a turns ratio of 1. The input and output voltages of the converter are shown in Fig.22 and Fig.23

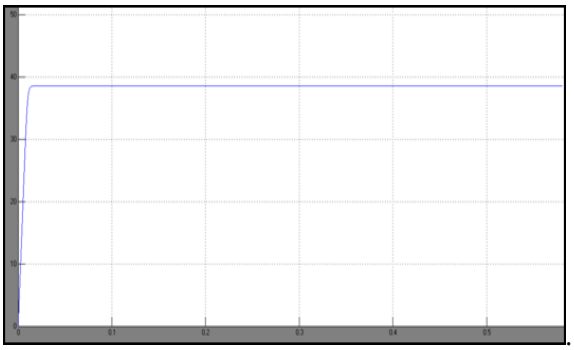

Fig.23. Input voltage of the boost converter

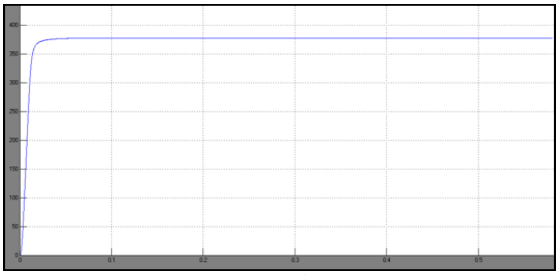

Fig.24. Output voltage of the boost converter

VI. HARDWARE DESCRIPTION

A prototype of the proposed converter is tested. The output obtained for the converter for an input of 12V is 150 V with a switching frequency of 50kHz. The converter is controlled by the microchip ATMEGA 16. The power supply unit for the driver board is shown in Fig.25. It uses the AC mains electricity as an energy source. It employs a transformer to convert the input voltage to a higher or lower AC voltage. A rectifier is used to convert the transformer output voltage to a varying DC voltage, which in turn is passed through an electronic filter to convert it to an unregulated DC voltage. The regulator are provided for the supply output of +5 V. The filter removes most, but not all of the AC voltage variations and the remaining voltage variations are known as ripple.

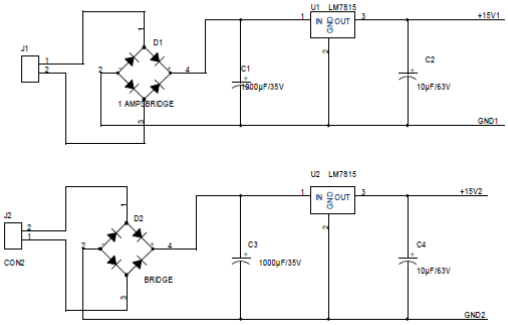

Fig.25. Driver board power supply

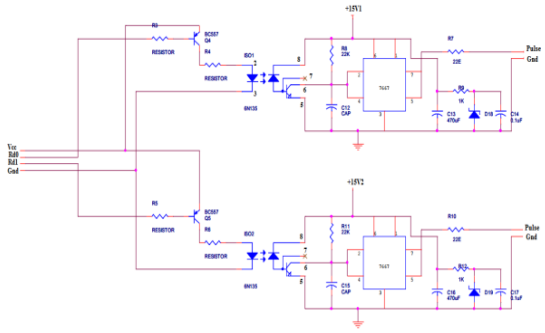

Fig.26. MOSFET Driver circuit

The power circuit for the micro controller is shown in Fig.27. It is provided with transformer, rectifier, regulator. The regulator are provided for the supply output of +5 V. The controller circuit are provided with oscillator and capacitors. The +5 V output from the power supply unit are used for V_{cc} of microcontroller.

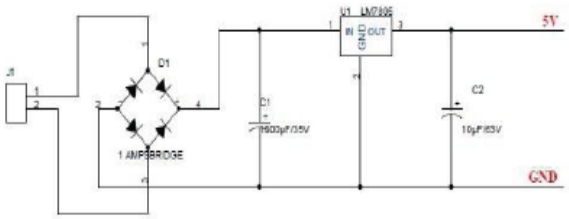

Fig.27. Controller circuit power supply

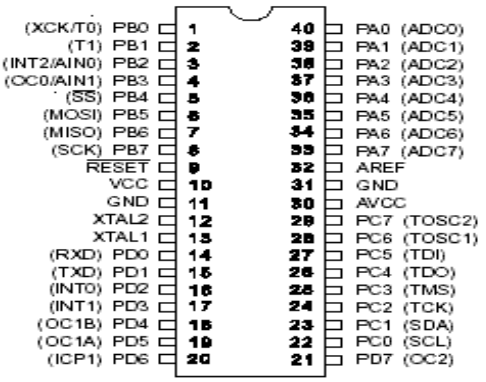

Fig.28. Pin diagram of ATMEGA 16

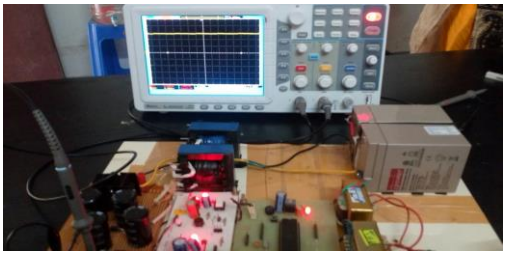

Fig.29. Experimental setup

VII. CONCLUSION

A novel high voltage gain interleaved boost converter with dual coupled inductors for high step up and high power applications is recommended for high voltage conversion. This configuration inherits the merits of high voltage gain, low output voltage ripple and low-voltage stress across the power switches. Moreover, the secondary sides of two coupled-inductors are connected in series to a regenerative capacitor by a diode for extending the voltage gain and balancing the primary-parallel currents. In addition, the active switches are turned on at zero-current and the reverse recovery problem of diodes is alleviated by reasonable leakage inductances of the coupled inductors. Besides, the energy of leakage inductances can be recycled. So the proposed system is suitable for renewable energy applications that need high step- up high power energy conversion.

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