A High Speed 2-D DWT Architecture using 9/7 Lifting Scheme for Image Compression

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Abstract—The Real-Time implementation for compression techniques plays an important role in optimizing the performance parameters such as speed, area etc. In this paper, we propose an FPGA Implementation of High Speed 2-D DWT using 9/7 lifting scheme for image compression. The 1-D DWT core architecture is implemented using signed multipliers which are required for representing floating-point coefficient values of 9/7 lift scheme. The proposed 2-D DWT architecture is designed efficiently using two 1-D DWT core, Memory Unit and Control Unit. The proposed 2-D DWT is extended for image processing application to compress the 2-D image which is synthesized using Virtex-5 xc5vlx110t-3ff1136 board. It is observed that the performance parameter with respect to operating speed of 232.823MHz is achieved compared to existing architectures.

Keywords—Discrete Wavelet Transform (DWT); Lifting Schemes; FPGA; LUTs; Image Compression.

I. INTRODUCTION

Image compression plays a vital role in reducing the bandwidth for real time data transmission. The Discrete Wavelet Transform (DWT) is being visualized as a major tool for image compression due to the fact that DWT has many useful properties like symmetrical transform, integer to integer transform, in-place computation, and progressive image transmission by resolution [1]. DWT understands Human Visual systems better so that it has been accepted in JPEG 2000 standard and adopted as the transform coder in MPEG-4 still texture coding. The conventional implementation using filter bank approach for 2-D DWT demands very high computation than the Discrete Cosine Transform (DCT) and demands more silicon area with power. Hence Swelden et al., [2] have suggested lifting based scheme. This method speeds up and reduces the computation compared to classical convolution.

The DWT has been vastly implemented in very-large scale integration (VLSI) to meet the real time specifications. Presently many VLSI architectures have been have been proposed based on lifting scheme. Sugreev Kaur et al., [3] proposed pipelined partially serial architecture to enhance the speed along with optimal utilization and resources available on target FPGA. This design can operate at maximum frequency 231 MHz in Spartan 3 FPGA by consuming power of 117mW at 28 degree/c junction temperature. Naseer et al., [4] proposed architecture based on lifting scheme approach, using the (5/3) wavelet filter, which reduces the hardware complexity and size of the on-chip memory. This architecture consists of a control unit, a processor unit, two on-chip internal memories to speed up system operations, and an on-board off-chip external memory (Intel strata parallel NOR flash PROM). It operates at maximum speed of 62.767 MHz on Spartan 3E FPGA. Eshwar Reddy and Venkata Narayanay [5] proposed a technique to compress the test images competitively by using Set Partitioning In Hierarchical Trees (SPIHT) algorithm and with lifting concepts. These algorithms resulted in practical advantages, such as, superior low bit rate performance, bit-level compression, progressive transmission by pixel, accuracy and resolution. Hansa et al., [6] proposed a highly pipelined and distributed VLSI architecture of lifting based 2D DWT with lifting coefficients represented in fixed point [2:14] format. Compared to conventional architectures, the highly pipelined architecture has high speed design at the expense of more hardware area.

Contribution:

In this paper, VLSI architecture for High Speed 2-D DWT using 9/7 Lifting Scheme for Image Compression is proposed. The architecture for 1-D DWT core, control unit and two memory module blocks are designed to obtain 2-D DWT.

The paper is organized as follows. Section II discusses the concept of the 9/7 lifting DWT. Section III presents the proposed architecture for 9/7 lift 2-D DWT. Results and discussions are given in section IV. Finally, in Section V brief conclusion is drawn.
II. 9/7 LIFTING SCHEME

The convolution method of finding filter coefficients is very slow and consumes high memory area. So, most of the recent architectures have utilized lifting based DWT for similar computation. There are three steps in 9/7 lifting [3] scheme: Splitting, Predict-Update and Scaling.

A. Split

The input data samples are divided into even and odd samples.

\[
Xe = X(2i) \quad \text{even samples} \tag{1} \\
Xo = X(2i+1) \quad \text{odd samples} \tag{2}
\]

B. Predict-Update

The odd sample is predicted using two even samples which obtains detailed coefficient. The average coefficients are updated using two detailed coefficients obtained. \(D(i)\) and \(S(i)\) are the detailed and average coefficients respectively.

Predictor1:

\[
D1(i) = Xo(i) + \alpha[Xe(i) + Xe(i + 1)] \tag{3}
\]

Updater1:

\[
S1(i) = Xe(i) + \beta[D1(i-1) + D1(i)] \tag{4}
\]

Predictor2:

\[
D2(i) = D1(i) + \gamma[S1(i) + S1(i + 1)] \tag{5}
\]

Updater2:

\[
S2(i) = S1(i) + \delta[D2(i-1) + D2(i)] \tag{6}
\]

Where, \(\alpha = -1.586134342\), \(\beta = -0.052980118\), \(\gamma = 0.882911076\), \(\delta = -0.443506852\), \(K = 1.149604398\)

C. Scaling

The low pass and high pass coefficients computed must be normalized before passing to the next stage. Scaling performs this operation, which reduce the hardware requirements as given in equation 7 and 8 respectively.

\[
YL(i) = K \times S2(i) \tag{7}
\]

\[
YH(i) = \frac{1}{K} \times D2(i) \tag{8}
\]

The general data flow diagram for 9/7 DWT is shown in Fig. 1. Filter coefficients are multiplied with input data samples in a pre-determined manner to get the high pass and low pass coefficients.

III. PROPOSED ARCHITECTURE

A. Proposed 1-D DWT Processor Core

The proposed 1-D DWT core architecture is as shown in Fig. 2. The design is very simple as it uses only four adders and six multipliers. The signed multipliers are designed since the filter coefficients of 9/7 filter have negative values. Once the multiplication is performed we extract only the desired part of the multiplication result and pass to the next stage. Similar to the multiplication, addition is also based on the signed operation.

B. Proposed 2-D DWT architecture

The Proposed 2-D DWT architecture is as shown in Fig. 3. It consists of two 1-D DWT core to implement 2-D DWT. The 1-D DWT core is explained in previous section.
The Data input INP from the image is fed to the 1-D DWT core through multiplexer (Mux) with DATA_CONTROL low. The Low pass (L_OP) and high pass coefficients (H_OP) output of 1-D DWT are passed to the memory units through De-multiplexer (Demux) and stored separately. Each memory unit size is $N^2/2$. The 1-D DWT data stored in both memory units are accessed in column-wise and passed to both 1-D DWT cores to calculate 2-D DWT. The speed of design is increased since all four sub-bands are calculated simultaneously.

### C. Control Unit

This unit is very important block in scheduling the operation of each module or block in the architecture. The detailed structure of control unit is shown in Fig. 4. It consists of only two counters, two multiplexers and a clock divider circuit. Clock Divider circuit divides the main clock frequency by value two. The output of Clock Divider is given as input to the first counter, Counter1. Counter1 counts till it reaches $N^2$ (where $N$ is the image size for $N \times N$) and this count value itself is address ADDR for the memory module to store the 1-D DWT coefficients. The RST_ON, DATA_CONTROL and Z are made high when the counter 1 value reaches $N^2$. RST_ON triggers the counter 2. The counter 2 starts counting and the output value of counter 2 is used as address to access the data from memory in column-wise to compute 2-D DWT coefficients. The controller unit is used to synchronize all the blocks in the proposed architecture of 2-D 9/7 Lift DWT using control signals.

### IV. RESULTS AND DISCUSSIONS

The proposed 9/7 lift based architecture is synthesized on Xilinx FPGA target device using Virtex-5 xc5vlx110t-3ff1136 with -3 Grade speed. The device utilization summary is shown in Table 1. It is observed that the proposed architecture utilize 632 slice registers and 18% of the slice LUTs available. It requires total memory of $N^2$. The simulation is performed in Xilinx ISE. The original uncompressed image and the compressed LL band are shown in Fig. 5 and Fig. 6 respectively. The Table 2 shows the comparison of proposed architecture with existing architectures in terms of adders, multipliers and registers. The Comparison with existing architecture in terms of slice registers, LUTs and speed for Virtex-5 is shown in Table 3.
TABLE 1. HARDWARE UTILIZATION

<table>
<thead>
<tr>
<th>Logic utilization</th>
<th>Used</th>
<th>Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice registers</td>
<td>632</td>
<td>69120</td>
</tr>
<tr>
<td>Number of Slice LUTs</td>
<td>12585</td>
<td>69120</td>
</tr>
<tr>
<td>Number of LUT-FF pairs</td>
<td>452</td>
<td>6435</td>
</tr>
<tr>
<td>Number of Bonded IOBs</td>
<td>53</td>
<td>640</td>
</tr>
<tr>
<td>Number of BUFG/BUFGCTRLs</td>
<td>4</td>
<td>32</td>
</tr>
</tbody>
</table>

TABLE 2. COMPARISON OF VARIOUS ARCHITECTURES WITH PROPOSED FOR 9/7 2-D DWT

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Adders</th>
<th>Multipliers</th>
<th>Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vidyadhar Gupta et al., [14]</td>
<td>8</td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>Yeong-kang Lai et al., [13]</td>
<td>16</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>Anand Darji et al., [15]</td>
<td>16</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>Bing-wei Wu et al., [17]</td>
<td>8</td>
<td>6</td>
<td>NA</td>
</tr>
<tr>
<td>Wei Zang et al., [16]</td>
<td>16</td>
<td>10</td>
<td>34</td>
</tr>
<tr>
<td>Proposed</td>
<td>8</td>
<td>12</td>
<td>2</td>
</tr>
</tbody>
</table>

TABLE 3. COMPARISON OF PROPOSED ARCHITECTURE WITH EXISTING ARCHITECTURE IN TERMS OF SLICES, LUT AND OPERATING FREQUENCY

<table>
<thead>
<tr>
<th>Architecture</th>
<th>LUT-FF pairs</th>
<th>Bonded IOB</th>
<th>BUFGs</th>
<th>Slice registers</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nagabhushanam et al., [18]</td>
<td>789</td>
<td>259</td>
<td>6</td>
<td>1152</td>
<td>180MHz</td>
</tr>
<tr>
<td>Proposed</td>
<td>452</td>
<td>53</td>
<td>4</td>
<td>632</td>
<td>232.823MHz</td>
</tr>
</tbody>
</table>
IV. CONCLUSION

In this paper, we propose an efficient architecture for 2D DWT computation based on 9/7 lifting scheme algorithm. The architecture uses two 1-D DWT core with processing blocks with reduced hardware resource utilization. Performance is high since all four sub-bands are calculated simultaneously. The architecture is synthesized using Xilinx ISE and targeted using Virtex-5 FPGA consisting of 110 million gates. The results obtained shows that the proposed design operates at maximum frequency of 232.823 MHz. The design occupies about 1% of the resource on FPGA.

REFERENCES


