A High Performance Energy-Efficient Architecture for Portable Wireless Devices based on Folded Tree and Multi-Bit Flip-Flop Merging Technique.

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Abstract— **Wireless data communication are an essential component of mobile computing with the help of wireless sensornodes. Due to their limited energy supply from batteries, the low power design have become inevitable part of today's wireless devices. Power has become a burning issue in VLSI design. In modern integrated circuits, the power consumed by clocking gradually takes a dominant part. Reducing the power consumption not only enhance battery life but also avoid overheating problem. By employing a more appropriate Processing Element(PE), the power consumption is significantly reduced. In this paper the novel method for low power design is achieved by using Folded Tree Architecture (FTA) and Multi-Bit Flip-Flop Merging (MBFM) technique for on-the-node data processing in wireless sensor networks using Parallel Prefix Operations (PPO) and data locality in hardware. Besides power reduction the objective of minimizing area and delay is also considered.**

Keywords— Folded Tree Architecture, Parallel Prefix Operation,Multi-Bit Flip-Flop Merging, Processing Element, Wireless SensorNetwork.

I. INTRODUCTION

Power optimization is always one of the most important design objectives in modern nanometer integrated circuit design. Especially for Wireless Sensor Networks (WSNs), power optimization have become inevitable part in today's VLSI design.Power optimization not only can enhance battery life but also reduce the overheating problem.

Self-configuring wireless sensor networks can be invaluable in many civil and military applications for collecting, processing, and disseminating wide ranges of complex environmental data. Because of this, they have attracted considerable research attention in last years. Sensor nodes are battery driven and hence operate on an extremely frugal energy budget. Further, they must have a lifetime on the order of months to years. Since battery replacement is not an option for networks with thousands of physically embedded nodes.In some cases, these networks may be required to operate solely on energy scavenged from the environment through seismic, photovoltaic or thermal conversion. This transforms energy consumption into the most important factor that determines sensor node lifetime [1].

The another important application in wireless sensor networks is event tracking, which has widespread use in applications such as security surveillance and wildlife habitat monitoring. Tracking involves a significant amount of collaboration between individual sensors to perform complex signal processing algorithms such as kalman filtering, Bayesian data fusion and coherent beamforming. This applications will require more energy for their processing.

In general Wireless Sensor Networkscan operate in four distinct mode of operation: Transmit, Receive, Idle and Sleep. An important observation in the case of most radios is that operating in Idle mode results in significantly high power consumption, almost equal to the power consumed in the Receive mode. The data-driven nature of WSN applications requires a specific low power data processing approach. By employing more appropriate Processing Element, the power consumption in all the four mode of operation will be reduced significantly.In present VLSI technology, reducing power consumption is an important issue. Especially for WSN, due to their limited battery lifetime the low power VLSI design is become inevitable for wireless commmunication. The goal of this paper is to design an low-energy Folded Tree and Multi-Bit Flip-Flop Merging technique for WSN nodes.

II. RELATED WORKS

In paper [2], the author proposed low-energy data processing architecture for WSN nodes using folded tree method. This paper identifies that many WSN applications employ algorithms which can be solved by using parallel prefix-sums. Therefore, an alternative architecture is proposed to calculated them energy-efficiently. It consists of several parallel Processing Elements structured as a folded tree.The folded tree method with parallel prefix operations reduces the number of processing element and memory bottleneck. Due to clock distribution for more flip-flops, it consumes

more clock power and also parallel prefix operations has high delay.

In paper [3], a novel method is proposed for low clock power consumption in WSN nodes. A previously derived clock energy model is briefly reviewed while a comprehensive framework for the estimation of system wide (chip level) and clock sub-system power as function of technology scaling is presented. This framework is used to study and quantify the impact that various intensifying concerns associated with scaling will have on clock energy and their relative impact on the overall system energy. This technology scaling method reduces clock power consumption (both static and dynamic), but due to large number of processing element- area, inverter chain, Power-Delay Product is increased.

III. PROPOSED SCHEME

Folded Tree Architecture with Parallel Prefix Operation is used to reduce the total number of Processing Elements in the VLSI design. By reducing the number of processing elements, the total area is reduced. Area is proportional to power, so power consumption is also reduced. But during processing and transmission of signals, the WSN nodes will consume more power. Especially for clock distribution nearly 70% power will be consumed. In order to optimize the power during clock distribution, multi-bit flip-flop merging technique using clock skew is added with Folded Tree Architecture.

A. Folded Tree Architecture

A straightforward binary tree implementation of Blelloch's approach costs a significant amount of area as ninputs require $p = n - 1$ PEs. To reduce area and power, pipelining can be traded for throughput. With a classic binary tree, as soon as a layer of PEs finishes processing, the results are passed on and new calculations can already recommence independently [8].

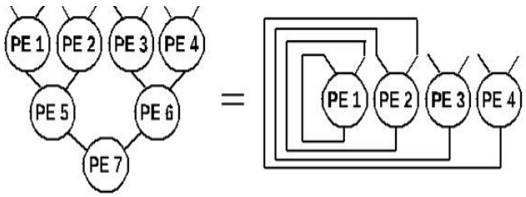

Fig 1. Binary tree equivalent to folded tree

The idea presented here is to fold the tree back onto itself to maximally reuse the PEs.In doing so, p becomes proportional to n/2 and the area is cut in half. Area is proportional to power, so power is also cut in half. Note that also the interconnect is reduced. This folded tree topology is depicted in Fig 1, which is functionally equivalent to the binary tree on the left.By using the Folded Tree architecture- power consumption, area and wirelength is reduced considerably.Folded Tree Architecture for on-the-node data processing in wireless sensor networks, using parallel prefix operations and data locality in hardware reduces both area and power consumption.

TABLE I
Leakage Power and Dynamic Energy for one PE under Normal Conditions

1 Processing Element	Active PE Core	Idle PE Core	PE instr. Mem.
Dynamic energy/Instr (pJ)	14.6	4.7	2.10
Leakage Power (µW)	0.03	0.03	0.01
Total Power @ 20MHZ (µW)	41.7	13.5	6.0

FTA is designed to reuse the PE nodes to reduce half of the total area. It limiting the data set by preprocessing with parallel prefix operations.The combination of data flow and control flow elements to introduce a local distributed memory, which removes the memory bottleneck while retaining sufficient flexibility.Several processing element consumes more power, so by using FTA the PE can be reused and power is reduced [2].

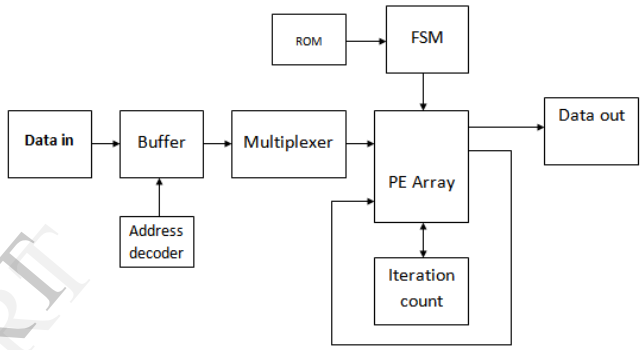

Fig 2. Folding Architecture

In folding architecture, we can reuse the PEs with the help of counter and Finite State Machine (FSM). Iteration count in the counter contains the total number of times the specified PE going to be reused. The FSM enables and reset the iteration count based on the instructions.

B. Parallel Prefix Adder

Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed.

The main idea behind parallel prefix addition is an attempt to generate all incoming carries in parallel and avoid waiting until the correct carry propagates from the stage of the adder where it has been generated. Parallel prefix adders are constructed out of fundamental carry operators denoted by ¢ as follows (G", P") ¢ (G', P') = (G"+G'·P", P'·P") where P" and P' indicate the propagations, G" and G' indicate the generations.

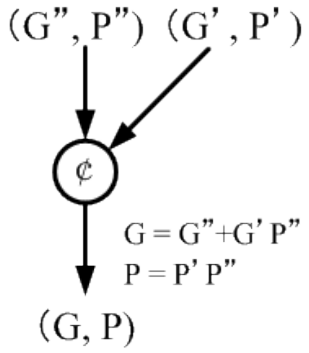

Fig 3. Carry operator

A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. The parallel prefix Ladner Fischer adder structure has minimum logic depth, but has large fan-out requirement up to n/2. Ladner Fischer adder has less number of delay compared to other parallel prefix adders. Power Delay Product should be less inorder to achieve high throughput and speed.

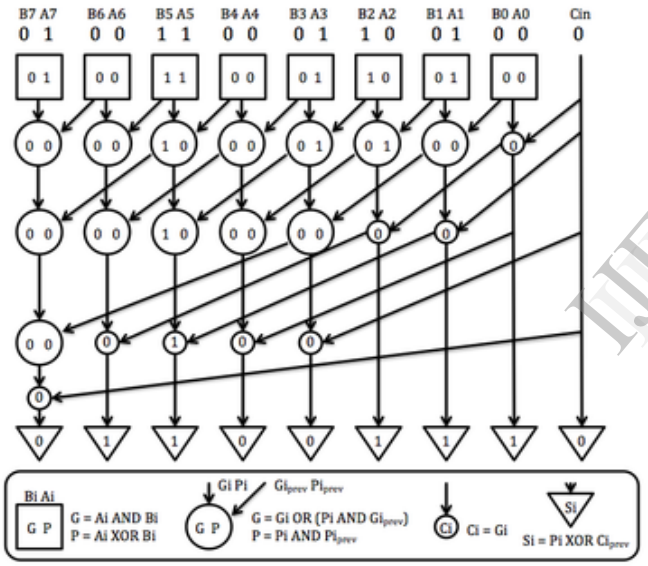

Fig 4. Ladner Fischer Parallel Prefix Adder

The Ladner Fischer adder construct a circuit that computes the prefix sums in the circuit, each node performs an addition of two numbers. With their construction, one can choose a tradeoff between the circuit depth and the number of nodes.

C. Multi-Bit Flip-Flop Merging Technique

Given a design that the locations of the cells have been determined, the power consumed by clocking can be reduced further by replacing several Flip-Flops (FFs) with multi-bit flip-flops. During clock tree synthesis, less number of flip-flops means less number of clock sinks. Thus, the resulting clock network would have smaller power consumption and uses less routing resource.

Besides, once more smaller flip-flops are replaced by larger multi-bit flip-flops, device variations in the corresponding circuit can be effectively reduced. As CMOS technology progresses, the driving capability of an inverter-based clock buffer increases significantly. Fig 5shows the block diagrams of 2 - and 4-bit flip-flops. The total power is reduced by merging the two 2- bit flip-flops with one4-bit flip-flops since the two flip flops consume the same clock [6].

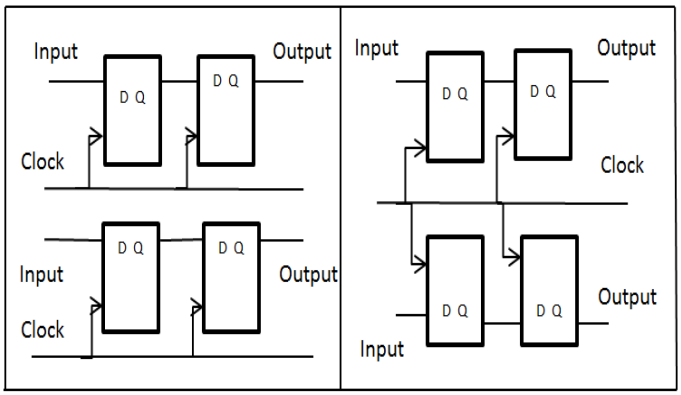

Fig 5. Flip-Flop Merging

1.Identify Mergeable flip-flops

Each and every flip-flops in the processing element have different clock skew. The clock skew is measured by calculating the delay difference between points having maximum and minimum delays.The rising skew is measured by calculating the time it takes for a signal to rise from 10% of Supply voltage to 90% of Supply voltage.

$$\text{Clock skew} = \text{Delay}_{Max} - \text{Delay}_{Min.} \quad (1)$$

$$\text{Rise Skew} = \text{Time}|_{v=0.9*Supply} - \text{Time}|_{v=0.1*Supply.} \quad (2)$$

The Falling skew is measured by calculating the time it takes for a signal to fall from 90% of Supply voltage to 10% of Supply voltage

$$\text{Fall Skew} = \text{Time}|_{v=0.1*Supply} - \text{Time}|_{v=0.9*Supply.} \quad (3)$$

Clock skew can be positive or negative. If the clock signals are in complete synchronicity, then the clock skew observed at these registers is zero.

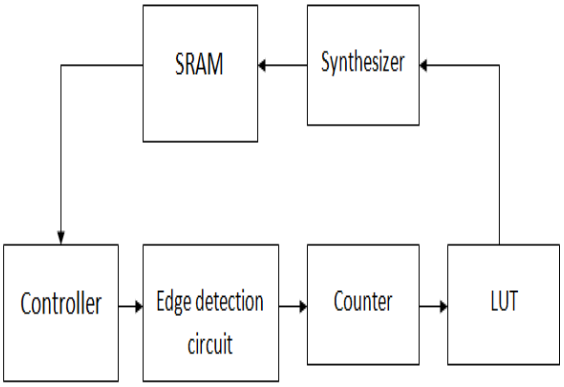

Fig 6. Multi-Bit Flip-Flop Merging technique

In this approach we are going to merge the flip flops with the help of clock skew. In the circuit the clock distribution for

each flip-flop has different clock skew to each other. The single-bit flip-flops having same clock skew are merged with each other to form single multi-bit flip-flops.For simulation we considered 20 regional clock signal, 50 flip-flops and 1 system clock. 20 regional clock signal supplied to 50 flip-flops, the skew difference between main and regional clock is identified by using edge detection circuit. We can use either rise edge or fall edge to measure skew difference. Here we used rise edge detection circuit. After finding the rise edge difference between system and regional clock, the counter counts the number of clock cycles between two clocks having same skew.

2. Build a Combination Table

Combination table is nothing but that contains each and every pair of mergeable flip-flops. The combination table, which records all possible combination of FFs to get feasible FFs before replacement. Only one combination of FFs needs to be considered in each time, the search time can be reduced greatly. Clock skew difference is used for building a combination table. In combination table, we use 50 flip-flops and 20 regional clock for simplicity. The combination table shows the FFs having same clock frequency, that can be merged by providing single clock.

3. Merge Flip-Flops

Clock signal distribution to large number of flip-flops in the circuit will consume most of the power from the power source. Instead of giving separate clock signal to each and every FFs in the circuit, we are going to give single clock signal to flip-flops based on the clock skew value generated from the combination table.Now, use the combination table to combine flip-flops in this subsection . Depending on the system clock and regional clock values, identify the flip-flops with same clock skew. The flip-flops those having same clock skew values are given single clock signal.

IV. SIMULATION RESULT

We simulated MBFM technique in ModelSim by considering 1 system clock, 20 regional clock and 50 flip-flops. We supplied 20 regional clock to 50 flip-flops and identified the skew difference between regional clock and system clock of each flip-flop separately. The skew difference for each and every flip-flop is built on the combination table.

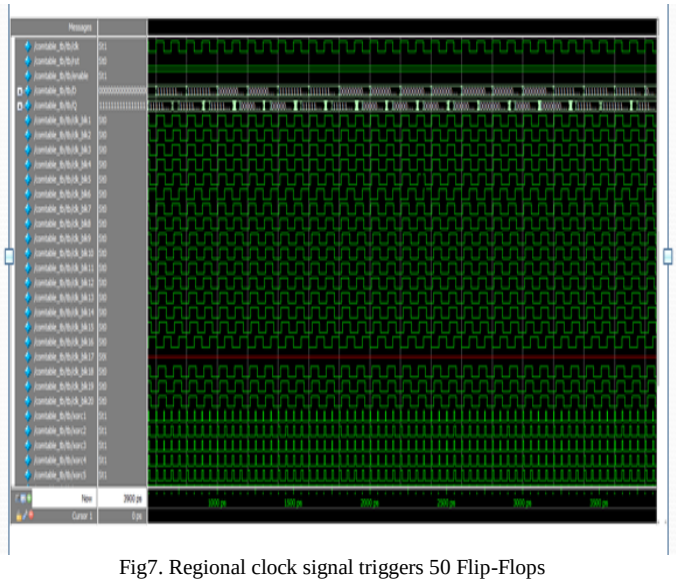

Fig7. Regional clock signal triggers 50 Flip-Flops

Clock distribution network triggers 50 Flip-Flops by using 20 regional clock signals.

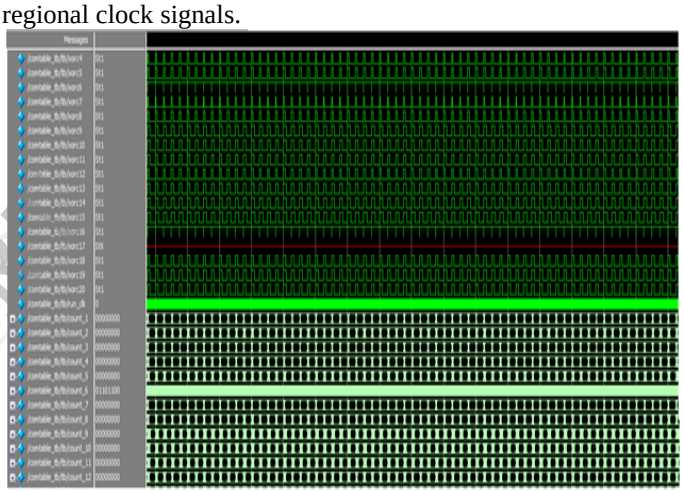

Fig 8. Edge detection by using differential circuit

Skew is detected by using differential Edge detection circuit. We use an exclusive OR gate to find out edges between various regional clock. Synchronous Clock signal directly to one input and skew clock is applied through a another part. It generates difference between system clock and regional clock. Here difference between main and distributed clocks is identified using xor array circuit. For MC = 0 and DC = 0, DS = 0, for MC = 0 and DC = 1, DS = 1, for MC = 1 and DC = 0, DS = 1 and for MC = 1 and DC = 1, DS = 0.

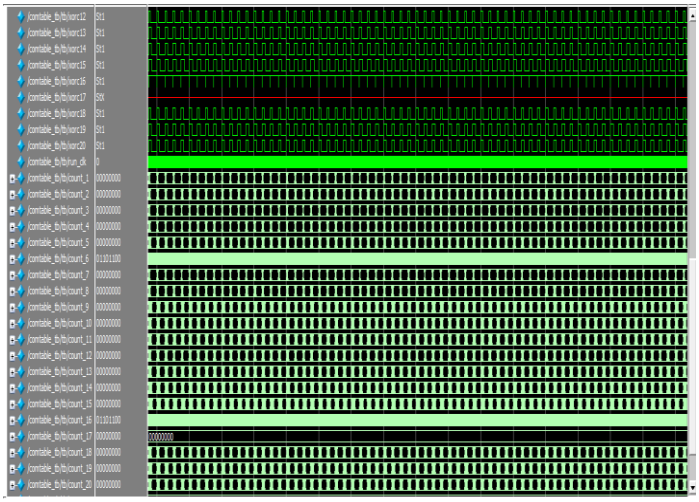

Fig 9. Counter values between clocks

The total rising edges occurs when there is difference between main clock and corresponding regional clock. Here we use 10 cyclic difference between reference clock and system clock. Initially counter variables are cleared by reset high and after one cycle period, it begin to count when edges are detected.

The combination table shows the flip-flops having same frequency, we merged the flip-flop by providing single clock signal. So power consumption of CDN is reduced by half.

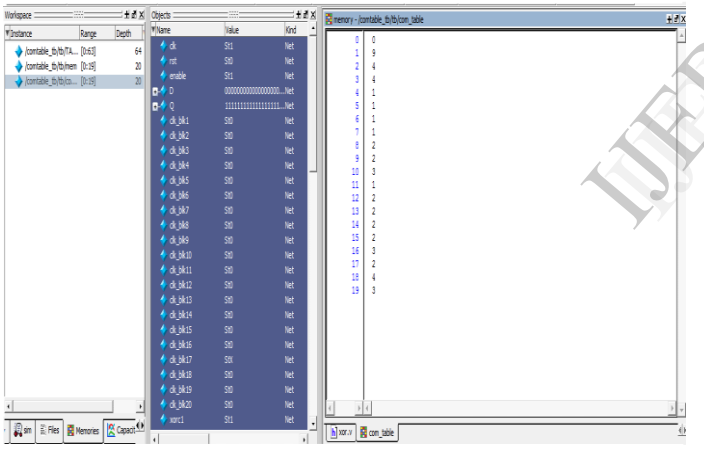

Fig 10. Combination Table

Combinational table memory obtained from ModelSim memory list analyzer. We are using 20 number of skew clocks distributed across 50 flip flops. Edge detection and counter circuit identifies total number of clock signals that operating under same frequency. From above look up table values, Clock 1 is used by 9 flip flop region where mergeable together. Clocks 4,5,6,7 are used by single flip flops that cannot be mergeable.

Altera quartus II 9 IDE is used for power analysis and throughput analysis. In power analysis, we observed that power consumption and area is reduced by the proposed method and throughput increased.

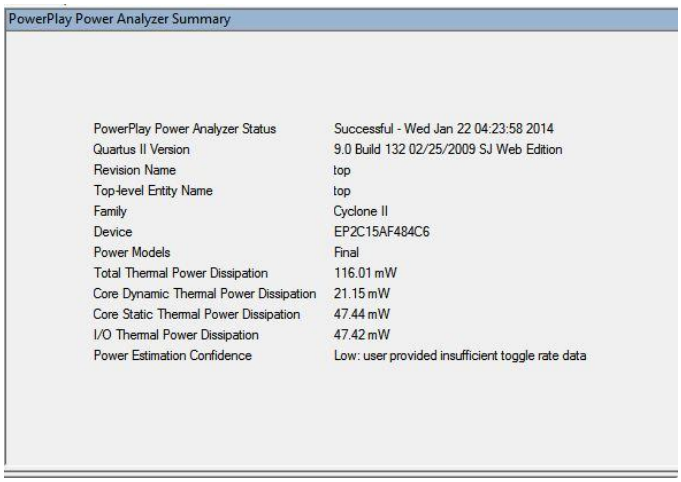

Fig 11. Power Analysis Report

Fig 11 power analysis results clearly shows the proposed system consumes less power compared to the existing system. It clearly shows the total thermal power consumption, dynamic power and I/O power consumption for the 50 flip-flops after implementing the proposed technique.The Fig 12 area analysis report shows that the total number of processing elements, registers, are reduced, so the total area usage is reduced.

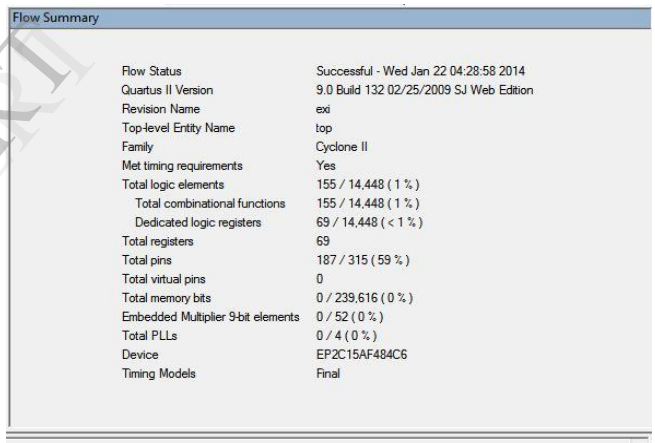

Fig 12. Area Analysis Report

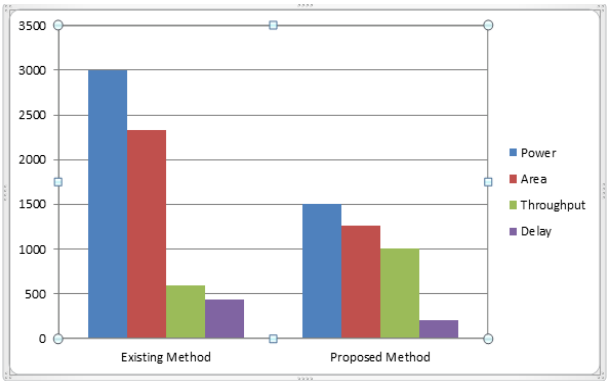

Fig 13. Comparsion of Existing and Proposed Methods

The proposed MBFM technique reduces power consumption from 128.12mw to 62.15mW, area utilization is reduced from 2334 logic elements from 1254 logic elements and delay by

325ns from 432ns. The throughput has been increased from 589Mbps to 325Gbps.

V. CONCLUSION

This paper presented the Folded Tree Architecture and Multi-Bit Flip-Flop Merging technique for WSN applications. The design describes many data processing algorithms for WSN applications along with parallel prefix operations and clock distribution networks. Power is saved using flip flop merging technique by providing single clock signal to mergeable flip flops with the help of combinational lookup table. Thus this technique can be effectively used in integrated circuits requiring low power consumption in clock distribution network and low skew clocks. Area is reduced using folded tree architecture by reusing processing element. Ladner Fischer parallel prefix adder reduces the delay constraints and achieve high throughput. The proposed architecture significantly reduces both power and area in WSN nodes, can save up to half of the power in total sensor node.

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