Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

A High Output Y-Source Boost DC/DC Converter for Renewable Applications

Kashapogu Arun
Department of Electrical and Electronics Engineering
G. Pulla Reddy Engineering College
Kurnool, Andhra Pradesh, India.

G. Kishor
Associate Professor
Department of Electrical and Electronics Engineering
Kurnool, Andhra Pradesh, India.

***Abstract* – Boost Dc/Dc converter based on Y-source impedance network with high gain without and with closed loop control is analyzed in this paper which provides solutions to distributed generation applications. The analyzed converter consists of a Y-source impedance network which has three-winding inductor tightly coupled for high voltage boosting which is indeed higher than the other classical impedance networks. Turns ratio and winding placement of this inductor can be designed to give the gain desired, while maintaining the duty ratio of switch smaller. Principle of operation is presented and analyzed by mathematical derivations and calculations. Analyzed converter is simulated using MATLAB and the results are in agreement with theoretical analysis and confirm the performance of analyzed converter.**

Key Words: Dc/Dc converter, Y-source, impedance network, closed loop control, PI controller.

I. INTRODUCTION

Distributed Generation powered by renewable energy sources like solar and fuel cells etc., have been gradually recognized as the reliable way of providing premium power for meeting energy demand in future for a low cost. Realizing such a distributed grid however requires more demanding power electronic converters for enhancing the low source voltages to a predefined grid voltage.

Consider fuel cells as an example, their power densities are comparably high, which along with their low emission and quiet operation, make them attractive as distributed sources [1]. However, the output DC voltages are low usually, and vary widely.

Converters with high voltage gains are thus needed generally for tying fuel cells to the distributed grid. Their ranges of gain variation must even be wide for tracking the wide output voltage variations of fuel cells.

It is hence important to style high gain converters for these sources, whose gains should ideally nullify the source variations before a regulated voltage are often obtained for grid interfacing. The converters that are designed should also match with other requirements of the intended sources, which for solar and fuel cells, are to avoid negative currents flowing into them and limit ripple currents drawn from them [2]. The converter types can be DC/DC, AC/AC, AC/DC or DC/AC depending upon the system requirement. For DC/DC converters, conventional boost [3], push-pull [4], half-bridge [5], full-bridge [6] and those with numerous voltage multiplier cells [7] have been tried for boosting low source voltages to a regulated DC-link voltage between 200V and 600V depending upon the system requirements.

The amount of boosting voltage, demands the inclusion of high frequency transformers in the converter circuits, whose turns ratios are increased proportionally with the demanded gains in almost all cases. The resulting turns ratios and total number of turns might therefore be high if high gain and satisfactory coupling are to be ensured simultaneously [6][8]. Alternatively, cascaded or multilevel techniques can be introduced to the converters for raising their gains but the number of components and complexity involved will undoubtedly increase.

Another way is to use two-winding coupled inductors for boosting voltage, whose turns ratios can be kept low comparably even at high gain voltage. Converters which are implemented with coupled inductors therefore can have higher power densities, as compared to the earlier mentioned methods.

The coupled inductors are different from the high-frequency transformers earlier mentioned since their magnetizing inductances are designed intentionally to be finite (ideally infinite for transformers). Based on this, a few magnetically coupled impedance networks have been found, whose origin dated back to the Z-source impedance network introduced in [9]. The Z-source network and its subsequent quasi [10] [11], embedded [12] [13] and series [14] variations use two inductors and two capacitors for voltage boosting. They have been demonstrated for DC/AC inverter [22], DC/DC converter [23], AC/AC converter [24] and AC/DC converter [25], but their gains are mentioned to be low. That has led to the development of the switched-inductor [15], tapped-inductor [16], cascaded [17], T-source [18], trans-Z-source [19], and TZ-source [20] networks.

The latter three networks are considered different from the others since they use magnetically coupled inductors for boosting gain. They are also different from those push-pull and bridge-based converters mentioned above in the way that their gains are increased at a rate faster than the usual proportional relationship with turns ratios. Their turns ratios and total number of turns can therefore be comparably lesser, while retaining the necessary magnetic coupling at higher power density. It is hence the intention of this paper to

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

continue by analyzing a Y-source network implemented as a high boost DC/DC converter [21].

The resulted converter uses a three-winding coupled inductor for flexibly deciding on its gain, which is presently not matched by any related converters. The number of components used is also kept small to allow the converter to be implemented compactly without compromising its performance. Y-source boost DC/DC converter without closed loop consists some error in the transient state.

To reduce this error closed loop controller is used. Results thus obtained are in match with theoretical analysis and confirm the performance expected from the converter.

II. Y-SOURCE IMPEDANCE NETWORK

The Y-Source impedance network is shown in Fig.1

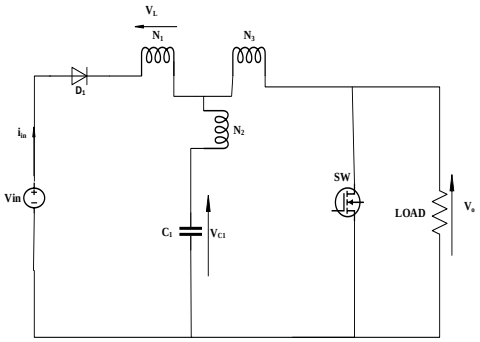

Fig. 1 Y-Source impedance network

It consists of an active switch SW, a passive diode D_1, a capacitor C_1 and a three-winding coupled inductor (N_1, N_2, N_3) for the high boost at a small duty ratio for switch SW. As the windings of the coupled inductor are connected directly to switch SW and diode D_1, its coupling should be tight to ensure very small leakage inductances at its winding terminals. For the Y-source inductor, three strings are wound to form three coupled windings inductor.

A. Circuit Analysis

(i) When the switch SW is turned ON, diode D_1 is reverse-biased, and replaced by an open-circuit in series with source. The equivalent circuit is as shown in Fig. 2.

By applying KVL, we have,

$$V_{C1} + \frac{V_L}{\left(\frac{N_1}{N_2}\right)} - \frac{V_L}{\left(\frac{N_1}{N3}\right)} = 0$$

$$\Rightarrow V_{C1} + \left(\frac{N_1}{N_2}\right) * V_L - \left(\frac{N_3}{N_2}\right) * V_L = 0$$

$$\Rightarrow V_{C1}(N_1) + V_L(N_2 - N_3) = 0$$

$$\Rightarrow V_L = V_{C1}\left(\frac{N_1}{N_3 - N_2}\right) \qquad (1)$$

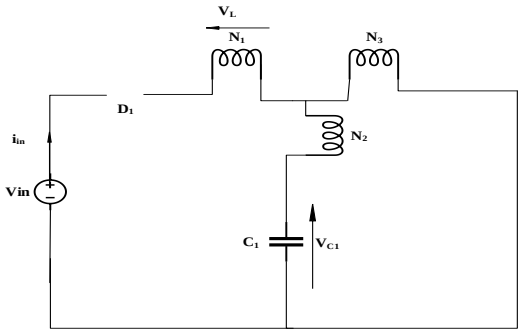

Fig. 2 Y-source impedance network equivalent during shoot through circuit

(ii) When the switch is turned OFF, the diode D_1 now conducts linking the source with the impedance network. The equivalent circuit is as shown in Fig. 3.

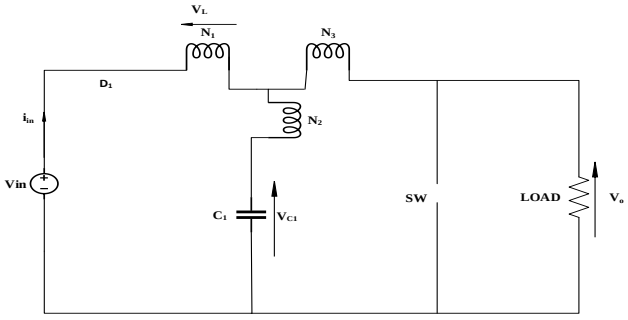

Fig. 3: Y-Source impedance network equivalent during non-shoot through circuit

By applying KVL, we have,

$$-V_{in} + \frac{V_L}{\left(\frac{N_1}{N_2}\right)} + V_L + V_{C1} = 0$$

$$\Rightarrow V_{in} = V_L\left(\frac{N_1 + N_2}{N_1}\right) + V_{C1}$$

$$\Rightarrow V_{in} - V_{C1} = V_L\left(\frac{N_1 + N_2}{N_1}\right)$$

$$\Rightarrow V_L = (V_{in} - V_{C1})\left(\frac{N_1}{N_1 + N_2}\right) \qquad (2)$$

Taking state space average of equations (1) and (2), we can get voltage across capacitor C_1,

$V_L(d_{ST}) + V_L(1 - d_{ST}) = 0$ (d_{ST} – normalized ON-time of switch SW)

$$\Rightarrow V_{C1} * \left(\frac{N_1}{N_3 - N_2}\right)(d_{ST}) + (V_{in} - V_{C1}) * \left(\frac{N_1}{N_1 + N_2}\right)(1 - d_{ST}) = 0$$

$$\Rightarrow V_{C1} * \left(\frac{N_1}{N_3 - N_2}\right)(d_{ST}) + \left(\frac{N_1}{N_1 + N_2}\right)(V_{in} - V_{in} * d_{ST} - V_{C1} + V_{C1} * d_{ST}) = 0$$

$$\Rightarrow V_{C1}\left[\left(\frac{N_1}{N_3 - N_2}\right)(d_{ST}) - \left(\frac{N_1}{N_1 + N_2}\right) + \left(\frac{N_1}{N_1 + N_2}\right) * d_{ST}\right] + V_{in}(1 - d_{ST})\left(\frac{N_1}{N_1 + N_2}\right) = 0$$

$$\Rightarrow V_{C1}\left[d_{ST}\left(\frac{N_1(N_1 + N_2) + N_1(N_3 - N_2)}{(N_3 - N_2)(N_1 + N_2)}\right) - \left(\frac{N_1}{N_1 + N_2}\right)\right] + V_{in}(1 - d_{ST})\left(\frac{N_1}{N_1 + N_2}\right) = 0$$

$$\Rightarrow V_{C1}\left[d_{ST}\left(\frac{N_1^2 + N_1 * N_2) + N_1 * N_3 - N_1 * N_2)}{(N_2 * N_3 + N_1 * N_3 - N_2^2 - N_1 * N_2)}\right) - \left(\frac{N_1}{N_1 + N_2}\right)\right] + V_{in}(1 - d_{ST})\left(\frac{N_1}{N_1 + N_2}\right) = 0$$

$$\Rightarrow V_{in}(1 - d_{ST})\left(\frac{N_1}{N_1 + N_2}\right) = V_{C1}\left[\left(\frac{N_1}{N_1 + N_2}\right) - d_{ST}\left(\frac{N_1(N_1 + N_3)}{(N_1 + N_2)(N_3 - N_2)}\right)\right]$$

$$\Rightarrow V_{in}(1 - d_{ST})(N_1) = V_{C1}[N_1(1 - d_{ST}(N_1 + N_3)]$$

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

$\Rightarrow$ Voltage across capacitor C_1, $V_{C1} = \left(\frac{V_{in}(1-d_{ST})}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right)$ (3)

We can find the peak output voltage V_o, from the non-shoot-through circuit as shown below:

$$-V_{in} + V_L + V_L\left(\frac{N_3}{N_1}\right) + V_o = 0$$

$$\Rightarrow \quad V_{in} = V_L\left(1+\frac{N_3}{N_1}\right) + V_o$$

Substituting equation (2) here, we get,

$$V_{in} = V_o + (V_{in} - V_{C1})\left(\frac{N_1}{N_1+N_2}\right)\left(1+\frac{N_3}{N_1}\right)$$

$$\Rightarrow \quad V_{in} = V_o + (V_{in} - V_{C1})\left(\frac{N_1}{N_1+N_2}\right)\left(\frac{N_1+N_3}{N_1}\right)$$

$$\Rightarrow \quad V_{in} = V_o + (V_{in} - V_{C1})\left(\frac{N_1+N_3}{N_1+N_2}\right)$$

$$\Rightarrow \quad V_{in} = V_o + V_{in}\left(\frac{N_1+N_3}{N_1+N_2}\right) - V_{C1}\left(\frac{N_1+N_3}{N_1+N_2}\right)$$

Substituting equation (3) here, we get,

$$\Rightarrow V_{in} = V_o + V_{in}\left(\frac{N_1+N_3}{N_1+N_2}\right) - \left(\frac{V_{in}(1-d_{ST})}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right)\left(\frac{N_1+N_3}{N_1+N_2}\right)$$

$$\Rightarrow V_{in} = V_o + V_{in}\left[\left(\frac{N_1+N_3}{N_1+N_2}\right) - \left(\frac{(1-d_{ST})}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right)\left(\frac{N_1+N_3}{N_1+N_2}\right) \right]$$

$$\Rightarrow V_{in} = V_o + V_{in}\left[\left(\frac{N_1+N_3}{N_1+N_2}\right)\left(1 - \left(\frac{(1-d_{ST})}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right)\right) \right]$$

$$\Rightarrow V_o = V_{in}\left[1 - \left(\frac{N_1+N_3}{N_1+N_2}\right)\left(1 - \left(\frac{(1-d_{ST})}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right)\right) \right]$$

$$\Rightarrow V_o = V_{in}\left[1 - \left(\frac{N_1+N_3}{N_1+N_2}\right)\left(- \left(\frac{d_{ST}\left(\frac{N_2+N_1}{N_3-N_2}\right)}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right)\right) \right]$$

$$\Rightarrow V_o = V_{in}\left[1 + \left(\frac{d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right) \right]$$

$\Rightarrow$ Peak output voltage, $V_o = V_{in}\left[1 + \frac{1}{1-d_{ST}\left(\frac{N_3+N_1}{N_3-N_2}\right)} \right]$

$\Rightarrow$ Peak output voltage, $V_o = V_{in}\left(1+\frac{1}{1-d_{ST}*K}\right)$ (4)

Where $K = \left(\frac{N_3+N_1}{N_3-N_2}\right)$, is a term introduced to represent the winding factor of the integrated magnetics.
Gain can be obtained from equation (4) as,

$$G_V = \frac{V_o}{V_{in}} = \left(1+\frac{1}{1-d_{ST}*K}\right) \quad (5)$$

Gain of the Y-Source network is raised exponentially by increasing its winding factor K. Different total number of turns needed by the Y-Source network for producing a higher voltage gain is also realized in the Table I.

TABLE I: Gain Of Y-Source Impedance Network For Different Winding Factor K And Turns Ratio (N_1:N_2:N_3)

$K = \left(\frac{N3+N1}{N3-N2}\right)$	$0 < d_{ST} < d_{ST,max}$	Gain, G_v	N_1:N_2:N_3
2	$0 < d_{ST} < 1/2$	$(1-2d_{ST})^{-1}$	1:1:3, 2:1:4, 1:2:5, 3:1:5, 4:1:6, 1:3:7
3	$0 < d_{ST} < 1/3$	$(1-3d_{ST})^{-1}$	4:2:5, 3:1:3, 2:2:4, 1:3:5, 4:3:5,

One can extend up to K=10 for different turns ratio (N_1:N_2:N_3) which obtain different gains.

III. Y-SOURCE BOOST DC/DC CONVERTER

For its high boost ability, the Y-source impedance network is suitable for implementing high gain converters like the high boost DC/DC converter.

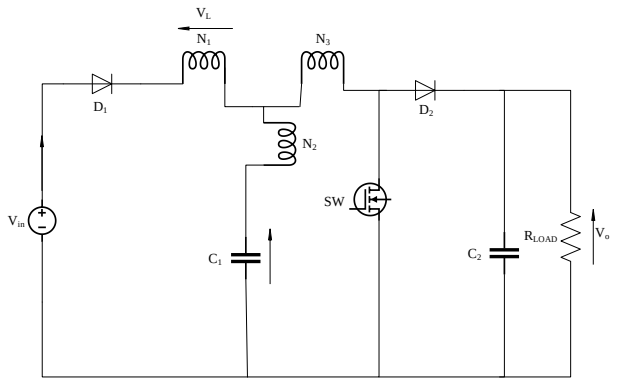

Fig. 4 Y-Source Boost Dc/Dc Converter

A. Principle of Operation

The Y-source boost DC/DC converter is as shown in Fig. 4, where only one controllable switch is used. In addition to the basic Y-source impedance network shown in Fig. 1, there is an extra diode D_2 and capacitor C_2 across load. Now, when the switch SW is turned on, diodes D_1 and D_2 will reverse-bias simultaneously. Then C_1 to charge the magnetizing inductance of the coupled inductor, and C_2 to power the load. Turning SW off, on the other hand, causes D_1 to conduct, and the input source to recharge C_1. The input source, together with the coupled inductor, also supplies energy to recharge C_2 and power the load, but only if the voltage V_o across capacitor C_2 is lower than voltage across switch SW. Then D_2 conducts, hence linking C_2 and the load to the rest of the circuit.

The same is repeated when SW turns on again. By periodically switching SW, the load voltage V_o across C_2 can be regulated, which according to equation (5) represents a gain of,

$$G_V = \frac{V_o}{V_{in}} = \left(1+\frac{1}{1-d_{ST}*K}\right)$$

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

This is the maximum gain that the Y-source network can provide.

B. Expected Operating Waveforms

Based on the operating principle described above, Fig. 5 shows some expected waveforms from the Y-source boost DC/DC converter in response to the applied gate-source voltage V_{GS} to switch SW.

When SW is on from t_0 to t_1 ($\Rightarrow d_{ST} = (t_1 - t_0)/T_S$), its drain-source voltage V_{DS} falls to zero, while its current I_{DS} increases to a finite value. That causes diodes D_1 and D_2 to become reverse-biased, and their voltages V_{D1} and V_{D2} to increase. The input current I_{in}, which is also same as the current I_{D1} through D_1, then collapses to zero during this interval.

When SW turns off at t_1, V_{DS} across it increases sharply, together with $I_{in} = I_{D1}$ and I_{D2} through the two diodes D_1 and D_2. These currents, in turn, charge capacitors C_1 and C_2 with voltage across C_2 increasing slightly above voltage across switch V_{SW} at t_2. When that happens, diode D_2 stops conducting with current across diode D_2, I_{D2} returned to zero. Since I_{D2} comes from the dc source, its reduction to zero also causes I_{in} to drop. The converter remains in this state until SW turns on again at t_3 ($\Rightarrow T_S = t_3 - t_0$), causing the waveforms to repeat the patterns. For I_{in} and I_{D2}, it should be mentioned that their patterns can change depending on the charging time constant of C_2. Longer charging time will increase the interval between t_1 and t_2, while a shorter charging time will reduce it. This variation however will not affect the maximum gain that is produced by the converter.

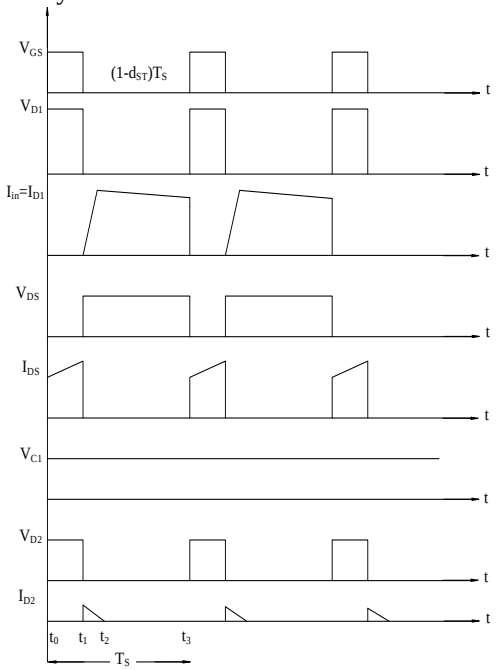

Fig. 5 Expected output waveforms from the Y-source boost DC/DC converter.

C. Design Parameters

Y-Source boost dc/dc converter is simulated using MATLAB for the turns ratio $N_1:N_2:N_3 = 3:1:5$.

$$\Rightarrow K = \left(\frac{N_3 + N_1}{N_3 - N_2}\right) = 2$$

And let $d_{ST} = 0.375$

For this we get gain as,

$$V_{C1} = \left(\frac{60(1-0.375)}{1-0.375\left(\frac{5+3}{5-1}\right)}\right)$$

$$G_V = \frac{V_o}{V_{in}} = \left(1 + \frac{1}{1 - d_{ST} * K}\right) = 4$$

Taking switching frequency, f = 12.6 KHz

From this time period, $T_S = 1/f = \left(\frac{1}{12.6*1000}\right) = 79.365\ \mu S$

We have $d_{ST} = \left(\frac{t_{on}}{t_{on} + t_{off}}\right) = \left(\frac{t_{on}}{T_S}\right)$

$\Rightarrow$ ON- time period, $t_{on} = d_{ST} * T_s = 0.375 * 79.365 = 29.761875\ \mu S$

And OFF-time period, $t_{off} = T_S - t_{on} = 79.365 - 29.761875 = 49.603125\ \mu S$

From equation (3), we know that voltage across capacitor C_1,

$$V_{C1} = \left(\frac{V_{in}(1 - d_{ST})}{1 - d_{ST}\left(\frac{N_3 + N_1}{N_3 - N_2}\right)}\right)$$

Substituting input voltage $V_{in} = 60V$, $d_{ST} = 0.375$ and $N_1:N_2:N_3 = 3:1:5$, we have,

$$\Rightarrow V_{C1} = \left(\frac{60(0.625)}{1 - 0.375 * 2}\right)$$

$$\Rightarrow V_{C1} = 150\ V.$$

Now from equation (1), we have,

$$V_L = V_{C1}\left(\frac{N_1}{N_3 - N_2}\right)$$

$$\Rightarrow V_L = V_{C1}\left(\frac{3}{5-1}\right)$$

$$\Rightarrow V_L = 112.5\ V$$

Therefore, voltage across inductor N_1,

$$V_{N1} = V_{L1} = V_L = 112.5\ V.$$

And voltage across inductor N_2,

$$V_{N2} = V_{L2} = V_L * \left(\frac{N_2}{N_1}\right) = 112.5 * \left(\frac{1}{3}\right) = 37.5\ V.$$

And voltage across inductor N_3,

$$V_{N3} = V_{L3} = V_L * \left(\frac{N3}{N_1}\right) = 112.5 * \left(\frac{5}{3}\right) = 187.5\ V.$$

We can similarly get inductance values as, $L_1 = 160.714\ \mu H$

$L_2 = 17.8571\ \mu H$

$L_3 = 446.428\ \mu H$

Generalized mutual inductance with three windings matrix is given as,

$$[L] = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix}$$

$$[L] = \begin{bmatrix} 160.714 & 53.57 & 267.85 \\ 53.57 & 17.8571 & 89.285 \\ 267.85 & 89.285 & 446.428 \end{bmatrix} * 1E\text{-}6\ H$$

The capacitance values are, $C_1 = C_2 = 470\ \mu F$ and the resistance is taken as load, $R_{LOAD} = 200$ ohms.

D. Simulation Results

The simulation results of Y-source boost dc/dc converter as follows:

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

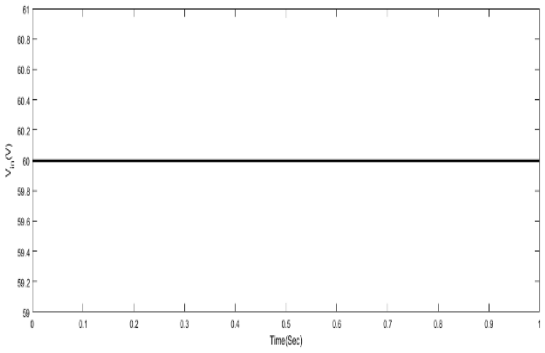

Fig. 6 Input voltage V_{in} = 60 V

Fig. 6 shows input voltage of V_{in} = 60 V which is given to the Y-Source boost DC/DC converter shown in Fig. 4.

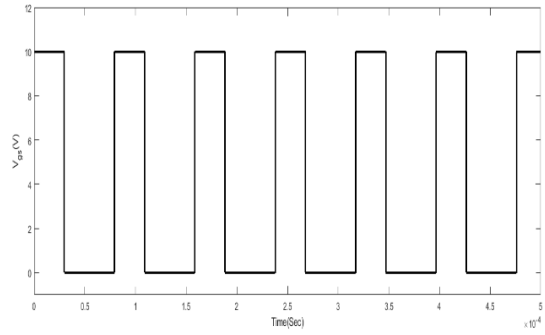

Fig. 7 Gate-Source Voltage V_{gs} (V)

Fig.7 shows gate-source voltage V_{gs} (V) with a duty ratio of 37.5% which has switching frequency of f_s=12.6 KHz (Time period, T_S = 79.365 µSec).

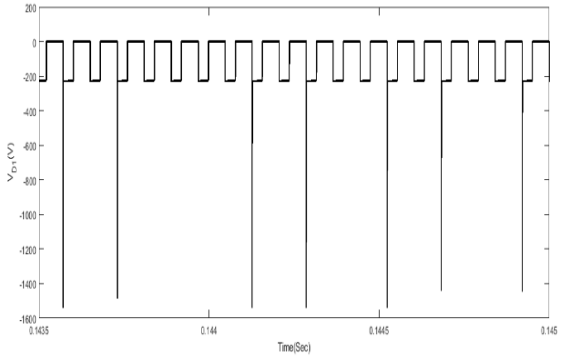

Fig. 8 Voltage across Diode D_1, V_{D1}(V)

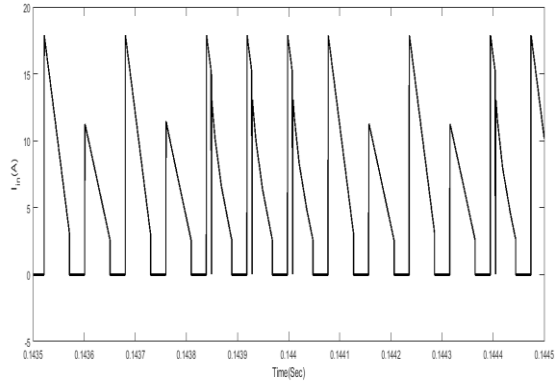

Fig. 9 Current through Diode D_1, $I_{D1} = I_{in}$(A)

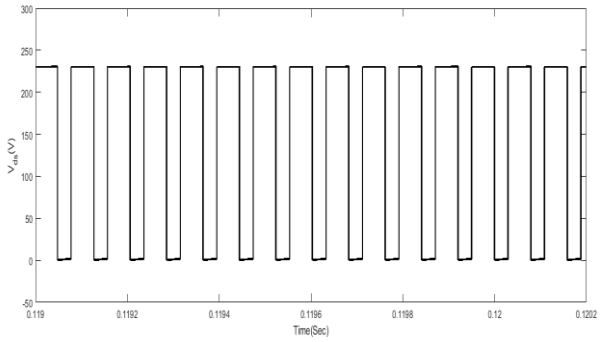

Fig. 10 Drain-Source voltage of SW, V_{ds}(V)

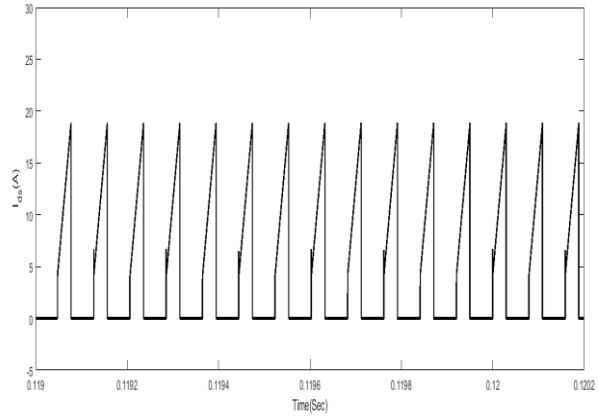

Fig. 11 Drain-Source current of SW, I_{ds}(A)

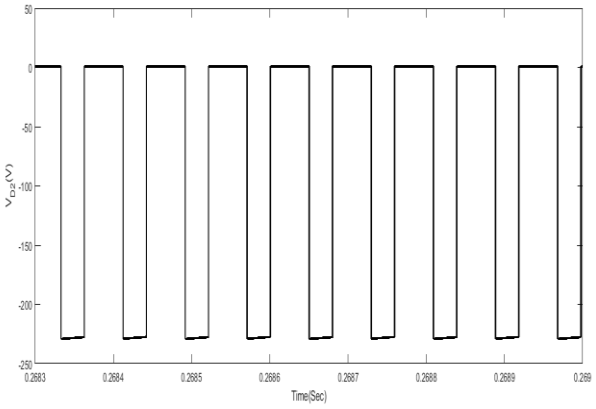

Fig. 12 Voltage across Diode D_2, V_{D2}(V)

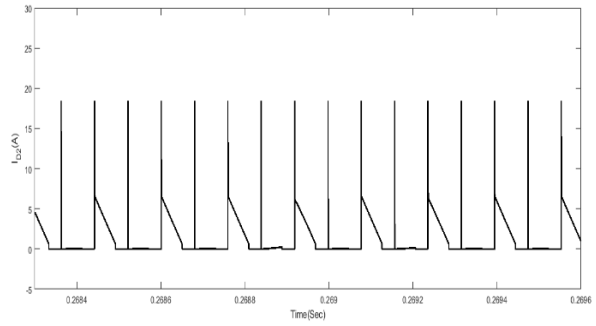

Fig. 13 Current through Diode D_2, I_{D2} (A)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

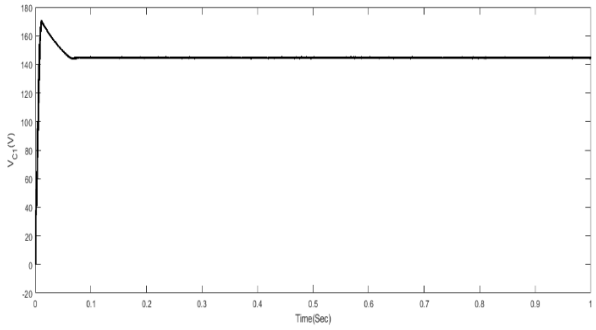

Fig. 14 Voltage across Capacitor C_2, V_{C1} (V)

Fig. 14 shows voltage across capacitor C_1, V_{C1} (V) which is approximately 150 V which supplies the voltage to converter shown in Fig.. 4 when the switch SW is turned off.

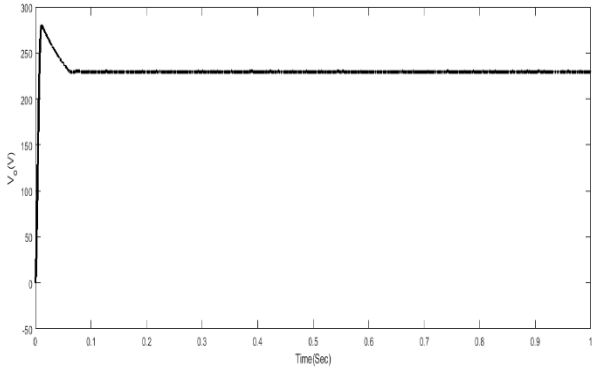

Fig. 15 Output voltage across R_{LOAD}, V_o (V)

Fig. 15 shows output voltage across R_{LOAD} = 200 ohms, V_o (V) which is around 230 V for an input voltage of V_{in} = 60 V with a gain of G_v = 3.83

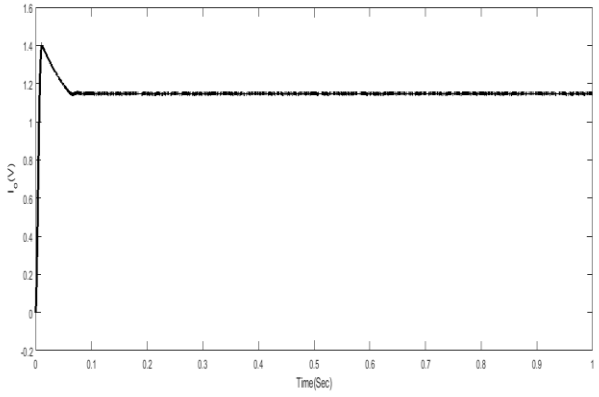

Fig. 16 Output current through R_{LOAD}, I_o (A)

Fig. 16 shows output current through R_{LOAD} = 200 ohms, I_o (A) which is 1.18 A with an output voltage of V_o = 230 V which gives output power $P_o = V_o * I_o$=271.4 W

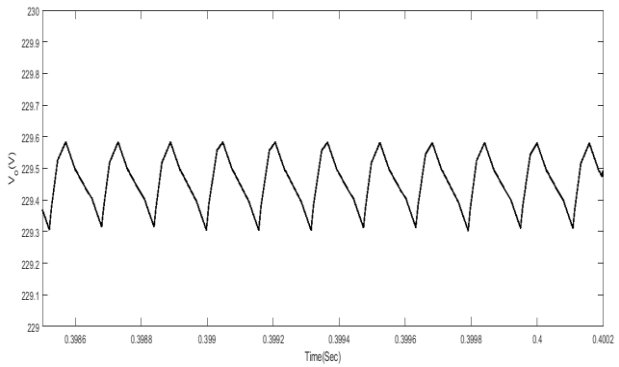

Fig. 17 Output ripple voltage across R_{LOAD}, V_o (V)

Fig. 17 shows output ripple voltage V_o(V) across R_{LOAD}, with a maximum ripple voltage of 229.6 V and a minimum ripple voltage of 229.3 V

$$\text{Normalized value of ripple voltage} = \frac{\text{Maximum value} - \text{Minimum value}}{\text{Average value}}$$

$$= \frac{229.6 - 229.3}{229.45}$$

$$= 0.001307$$

These are some of the tables evaluated for different load resistance, duty ratio and line voltage values to analyze the operation of the converter which are shown in TABLES II, III and IV.

TABLE II: LOAD REGULATION (V_{in}= 60 V)

Resistance, R (ohm)	Output voltage, V_o (V)	Output current, I_o (A)	Output power, $Po=V_o*I_o$ (W)
200	229.5	1.147	263.236
190	229.2	1.208	276.873
180	229.0	1.272	291.288
210	230.0	1.095	251.850

From the TABLE II, it is observed that, output power is increased when load value is decreased and the output power is decreased when the load is decreased by keeping input voltage (V_{in}= 60 V) constant.

TABLE III: DUTY RATIO REGULATION (V_{in}= 60 V)

Duty ratio, D	Output voltage, V_o (V)	Output current, I_o (A)
37.5	229.5	1.147
40.0	282.0	1.410
42.5	363.0	1.815
45.0	492.5	2.465
47.5	650.0	3.250

From the TABLE III, it is observed that, with increase in duty ratio, both output voltage and output current are increased by keeping both input voltage (V_{in}= 60 V) and load (R = 200 Ohms) constant.

TABLE IV: LINE REGULATION (R= 200 ohms)

Input voltage, V_{in} (V)	Output voltage, V_o (V)	Output current, I_o (A)	Output power, $P_o=V_o * I_o$ (W)
60	229.5	1.147	263.23
70	268.5	1.345	361.13
50	190.5	0.953	181.54

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

From TABLE IV, it is observed that, when input voltage is increased by keeping load resistance constant, the output power is increased and when input voltage is decreased, the output power is decreased by keeping load (R = 200 Ohms) constant.

From Figs. 15 and 16 one can observe that output voltage and current waveforms takes some time in transient state to settle. To reduce this rise time and improve the performance of the converter, closed loop control (PI controller) method is implemented by trial and error and simulated using MATLAB.

IV. CLOSED LOOP Y-SOURCE BOOST DC/DC CONVERTER USING PI CONTROLLER

Closed loop Y-source DC/DC converter using PI controller circuit diagram is as shown in Fig. 18:

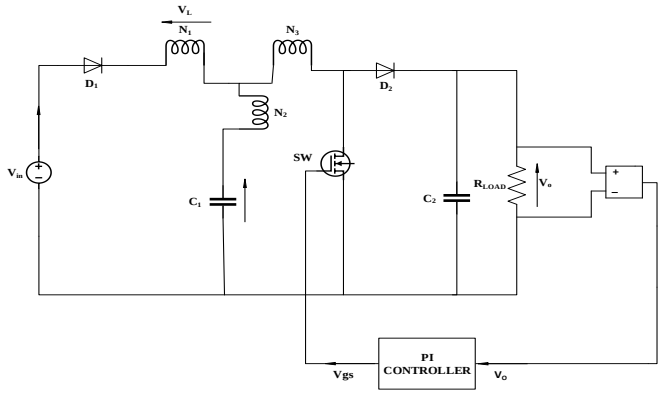

Fig. 18 Closed loop Y-source boost dc/dc converter using PI controller

PI controller used is as shown in Fig. 19:

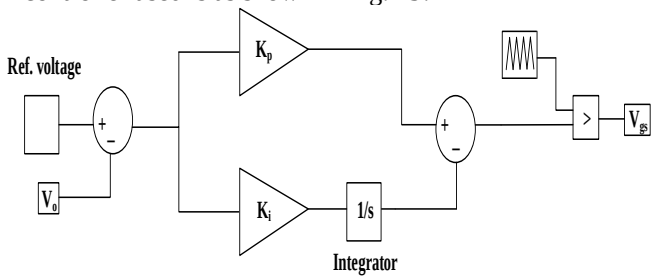

Fig. 19 PI controller used in Fig.18

The output voltage which takes more time to settle and the required reference voltage both are implemented using PI controller to reduce the error. And the resultant signal is compared with repeating sequence to generate the required pulse signal. This generated pulse signal is given to the gate terminal of the switch SW. Here reference voltage is 240 V and proportional constant K_p=0.75 and integral constant K_i=110.

A. Simulation Results

Now the results obtained for Y-source boost dc/dc converter using PI controller are as follows:

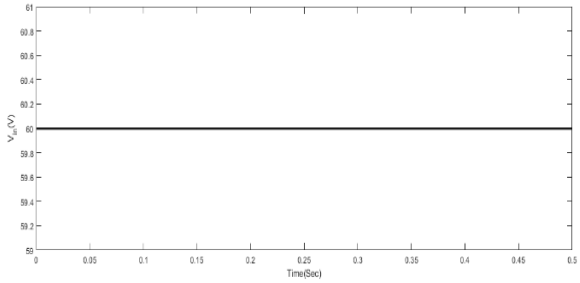

Fig. 20 Input voltage, V_{in} = 60 V.

Fig. 20 shows input voltage of V_{in} = 60 V which is given to the closed loop Y-Source boost DC/DC converter using PI controller shown in Fig. 18.

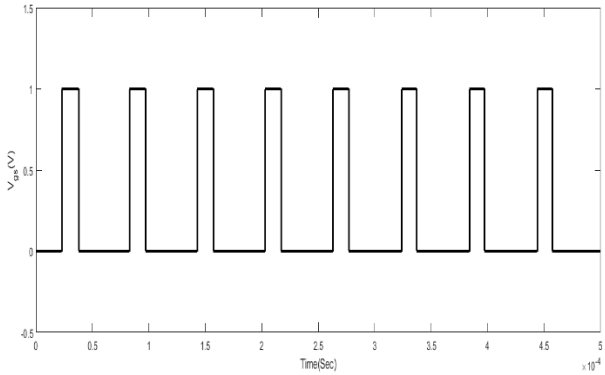

Fig. 21 Gate-source voltage of SW, V_{gs}(V)

Fig. 21 shows gate-source voltage of SW, V_{gs}(V) which is generated by using PI controller shown in Fig. 19.

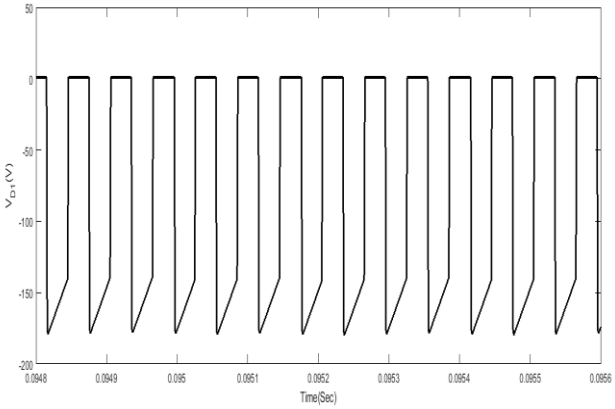

Fig. 22 Voltage across diode D_1, V_{D1}(V)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

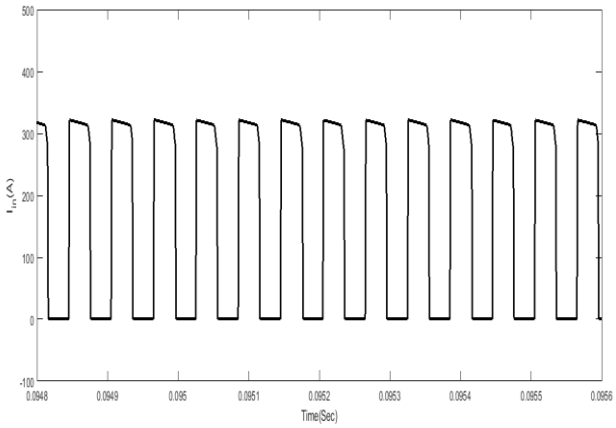

Fig. 23 Current through diode D_1, $I_{D1} = I_{in}$ (A)

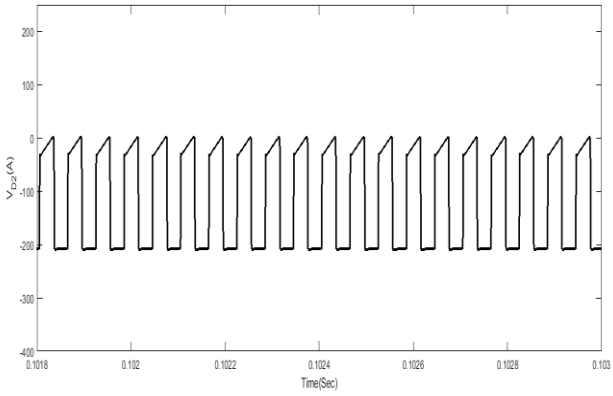

Fig. 24 Voltage across diode D_2, V_{D2}(V)

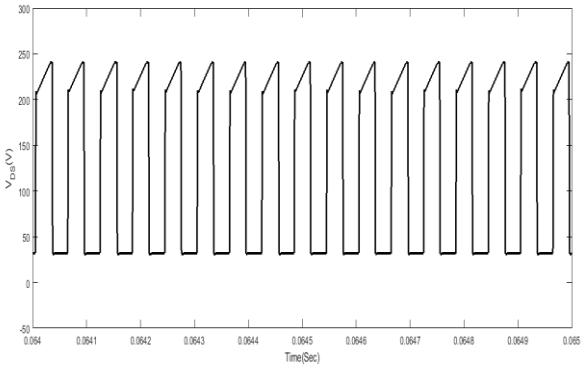

Fig. 25 Drain-source voltage of SW, V_{ds}(V)

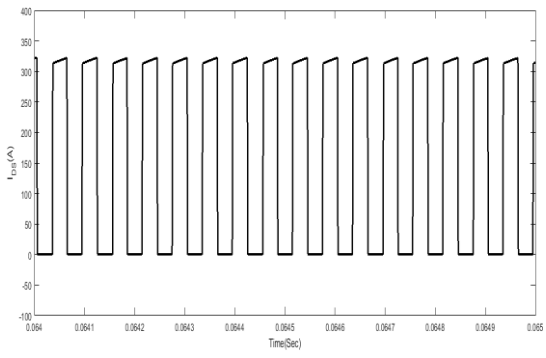

Fig. 26 Drain-source current of SW, I_{ds}(A)

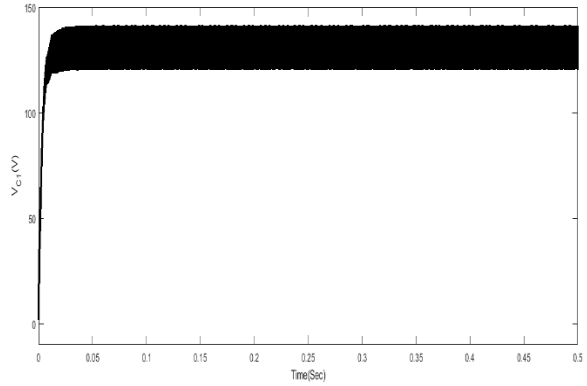

Fig. 27 Voltage across capacitor C_1, V_{C1}(V)

Fig. 27 shows voltage across capacitor C_1, V_{C1}(V) which is approximately 150 V which supplies voltage to the converter shown in Fig.18 when the switch SW is turned off.

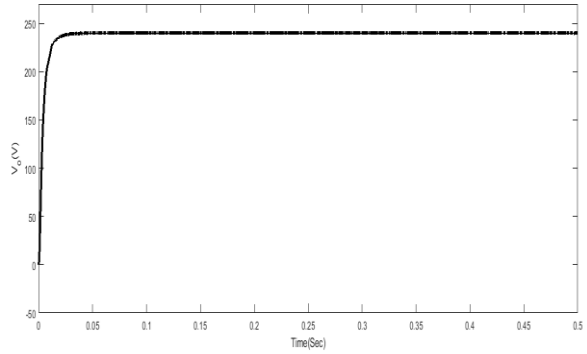

Fig. 28 Output voltage across R_{LOAD}, V_o(V)

Fig. 28 shows output voltage V_o(V) across R_{LOAD} = 200 ohms, which is 240 V for an input voltage of V_{in} = 60 V with a gain of G_v = 4.

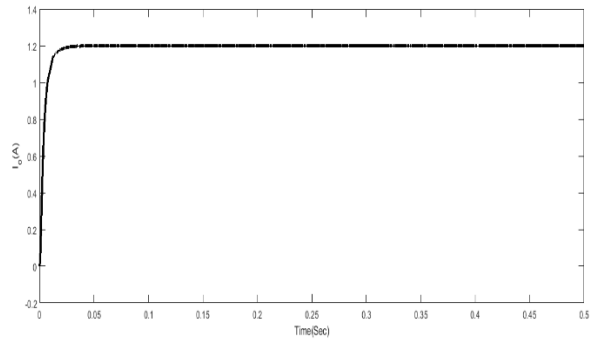

Fig. 29: Output current through R_{LOAD}, I_o(A)

Fig. 29 shows output current I_o(A) through R_{LOAD} = 200 ohms, which is 1.2 A with an output voltage V_o = 240 V which gives output power as $P_o = V_o * I_o$ = 288 W.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

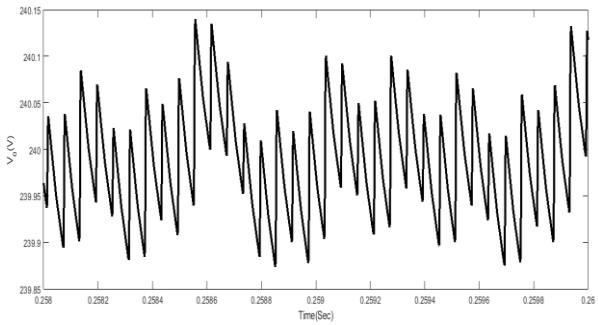

Fig. 30 Output ripple voltage across $R_{LOAD,}$ V_o(V)

Fig. 30 shows output ripple voltage V_o(V) across $R_{LOAD,}$ with a maximum ripple voltage of 240.04 V and a minimum ripple voltage of 239.85 V

$$\text{Normalized valueof ripple voltage} = \frac{\text{Maximum value - Minimum value}}{\text{Average value}}$$

$$= \frac{240.04 - 239.85}{239.945}$$

$$= 0.000791$$

By comparing the output voltage of Y-source boost dc/dc converter without and with closed loop control, one can observe that the spike obtained of output voltage in transient state is drastically reduced.

Similarly, for output current also the spike obtained of output current in transient state is improved.

And the ripples obtained in output voltage Y-source boost dc/dc converter without closed loop control are also reduced in output voltage by using closed loop control (PI controller).

V. CONCLUSION

A high gain DC/DC converter operating with a small switch duty ratio has been analyzed and simulated using MATLAB to validate the concept. The analyzed converter uses a Y-source impedance network consisting a three-winding coupled inductor. Turns ratio and winding placement of this inductor can be designed in a way to get the gain desired, while maintaining the duty ratio of switch smaller. The converter is thus unique with more degrees of freedom for tuning the gain, when compared to the existing coupled-inductor-based converters.

Therefore, boost dc/dc converter with high-gain which is based on Y-source impedance network without and with closed loop control have been analyzed providing solution to high voltage gain applications, for example in distributed generation.

REFERENCES

[1] S. Njoya Motapon, L. Dessaint and K. Al-Haddad, "A Comparative Study of Energy Management Schemes for a Fuel-Cell Hybrid Emergency Power System of More-Electric Aircraft," in IEEE Transactions on Industrial Electronics, vol. 61, no. 3, pp. 1320-1334, March 2014, doi: 10.1109/TIE.2013.2257152.

[2] Fuel Cell Handbook, 6th Edition, DOE/NETL-2002/1179, US Dept. of Energy, pp. 8.27-8.29, Nov. 2002.

[3] B. Huang, A. Shahin, J. P. Martin, S. Pierfederici and B. Davat, "High voltage ratio non-isolated DC-DC converter for fuel cell power source applications," 2008 IEEE Power Electronics Specialists Conference, Rhodes, 2008, pp. 1277-1283, doi: 10.1109/PESC.2008.4592107.

[4] G. K. Andersen, C. Klumpner, S. Kjaer and F. Blaabjerg, "A New Power Converter for Fuel Cells with High System Efficiency," *Int. J. Electron.*, vol. 90, no. 11/12, pp. 727-750, Nov. 2003.

[5] F. Z. Peng, Hui Li, Gui-Jia Su and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application," in IEEE Transactions on Power Electronics, vol. 19, no. 1, pp. 54-65, Jan. 2004, doi: 10.1109/TPEL.2003.820550.

[6] Jin Wang, F. Z. Peng, J. Anderson, A. Joseph and R. Buffenbarger, "Low cost fuel cell converter system for residential power generation," in IEEE Transactions on Power Electronics, vol. 19, no. 5, pp. 1315-1322, Sept. 2004, doi: 10.1109/TPEL.2004.833455.

[7] Y. J. A. Alcazar, D. de Souza Oliveira, F. L. Tofoli and R. P. Torrico-Bascopé, "DC–DC Nonisolated Boost Converter Based on the Three-State Switching Cell and Voltage Multiplier Cells," in IEEE Transactions on Industrial Electronics, vol. 60, no. 10, pp. 4438-4449, Oct. 2013, doi: 10.1109/TIE.2012.2213555.

[8] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg and G. E. Town, "Effects of leakage inductances on magnetically-coupled impedance-source networks," 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, 2014, pp. 1-7, doi: 10.1109/EPE.2014.6910982.

[9] Fang Zheng Peng, "Z-source inverter," in IEEE Transactions on Industry Applications, vol. 39, no. 2, pp. 504-510, March-April 2003, doi: 10.1109/TIA.2003.808920.

[10] J. Anderson and F. Z. Peng, "Four quasi-Z-Source inverters," 2008 IEEE Power Electronics Specialists Conference, Rhodes, 2008, pp. 2743-2749, doi: 10.1109/PESC.2008.4592360.

[11] J. Anderson and F. Z. Peng, "A Class of Quasi-Z-Source Inverters," 2008 IEEE Industry Applications Society Annual Meeting, Edmonton, AB, 2008, pp. 1-7, doi: 10.1109/08IAS.2008.301.

[12] Poh Chiang Loh, Feng Gao, Frede Blaabjerg and Ai Lian Goh, "Buck-boost impedance networks," 2007 European Conference on Power Electronics and Applications, Aalborg, 2007, pp. 1-10, doi: 10.1109/EPE.2007.4417391.

[13] P. C. Loh, F. Gao and F. Blaabjerg, "Embedded EZ-Source Inverters," in IEEE Transactions on Industry Applications, vol. 46, no. 1, pp. 256-267, Jan.-feb. 2010, doi: 10.1109/TIA.2009.2036508.

[14] Y. Tang, S. Xie and C. Zhang, "An Improved Z-Source Inverter," in IEEE Transactions on Power Electronics, vol. 26, no. 12, pp. 3865-3868, Dec. 2011, doi: 10.1109/TPEL.2009.2039953.

[15] M. Nguyen, Y. Lim and G. Cho, "Switched-Inductor Quasi-Z-Source Inverter," in IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3183-3191, Nov. 2011, doi: 10.1109/TPEL.2011.2141153.

[16] D. Li, P. C. Loh, M. Zhu, F. Gao and F. Blaabjerg, "Enhanced-Boost Z-Source Inverters with Alternate-Cascaded Switched- and Tapped-Inductor Cells," in IEEE Transactions on Industrial Electronics, vol. 60, no. 9, pp. 3567-3578, Sept. 2013, doi: 10.1109/TIE.2012.2205352.

[17] D. Li, F. Gao, P. C. Loh, M. Zhu and F. Blaabjerg, "Hybrid-Source Impedance Networks: Layouts and Generalized Cascading Concepts," in IEEE Transactions on Power Electronics, vol. 26, no. 7, pp. 2028-2040, July 2011, doi: 10.1109/TPEL.2010.2101617.

[18] R. Strzelecki, M. Adamowicz, N. Strzelecka and W. Bury, "New type T-Source inverter," 2009 Compatibility and Power Electronics, Badajoz, 2009, pp. 191-195, doi: 10.1109/CPE.2009.5156034.

[19] W. Qian, F. Z. Peng and H. Cha, "Trans-Z-Source Inverters," in IEEE Transactions on Power Electronics, vol. 26, no. 12, pp. 3453-3463, Dec. 2011, doi: 10.1109/TPEL.2011.2122309.

[20] M. Nguyen, Y. Lim and Y. Kim, "TZ-Source Inverters," in IEEE Transactions on Industrial Electronics, vol. 60, no. 12, pp. 5686-5695, Dec. 2013, doi: 10.1109/TIE.2012.2229678.

[21] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, S. J. Andreasen and G. E. Town, "Y-Source Boost DC/DC Converter for Distributed Generation," in IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 1059-1069, Feb. 2015, doi: 10.1109/TIE.2014.2345336.