A EV Battery Charger Using a PFC based Bridgeless SEPIC Converter

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***Abstract*—Conventional PFC circuits in EV (Electric Vehicle) battery chargers have the efficiency limitation. To overcome this issue,their were lossess associated with thw DBR,hence a bridgeless single ended primary inductance converter (SEPIC) with improved power quality is presented in this paper. Input current drawn by the charger shows a unity power factor operation in a complete switching cycle. Due to elimination of DBR, conduction losses are significantly controlled. The overall performance of the proposed bridgeless SEPIC converter is analysed with the help of various operating modes.The battery is charged at constant current/ constant voltage control mode and it provides satisfactory results for inherent power factor correction, thus, improving overall performance of the charger.**

Keywords— Electric Vehicle; Bridgeless system SEPIC Converter; Diode bridge rectifier (DBR); Power Quality; Constant Current/Constant Voltage (CC/CV) control

I. INTRODUCTION

The recent and upcoming vehicle technology comprises an energy storage system known as BESS (Battery Energy Storage System), which charging system incorporates certain power electronic interfacing circuit as illustrated. These power electronics circuits that regulate the charging voltage for BESS, should be designed efficient enough to maintain international power quality (PQ) standards at the input side of the AC-DC converter, as given. Being a key component of an EV charger, the front-end PFC converter should be designed to achieve the efficiency and size goals along with inherent unity power factor operation. In order to have maximum power supply efficiency, lots of efforts have been made in literature to design bridgeless PFC converter topologies which reduces switches conduction loss by eliminating the diode bridge rectifier (DBR) and thus, making the current to flow through less number of semiconductor switches. For power factor correction, conventional boost converter, with diode bridge, has been the foremost choice in power electronics equipment but at high power levels, boost converters involve some severe issues like converter efficiency degrades due to increased bridge losses, increased size of inductor and increased high frequency ripple in DC link capacitor if a low value of inductor is selected.. A comprehensive study of various single phase AC-DC PFC converters has been discussed in with their procedures, and control techniques employed and performance verification in different applications. Because of low conduction losses, reduce input current ripple, good efficiency at low level of input voltage and lower switch voltage stress.

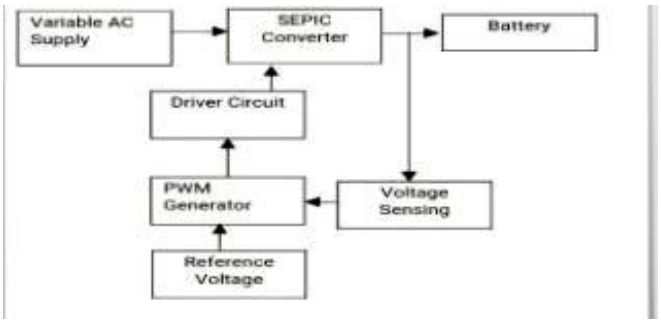

Fig. 1. Block diagram of A EV Battery Charger Using a PFC based Bridgeless SEPIC Converter

II. BRIDGELESS ISOLATED SEPIC PFC CONVERTER FOR BATTERY CHARGING.

The proposed system configuration for EV battery charger, as shown in Fig.1, incorporates two SEPIC isolated converters to be operated in alternate cycles of supply voltage, one at a time. An input DBR is eliminated at the input so that conduction losses associated with the switching devices are significantly reduced.

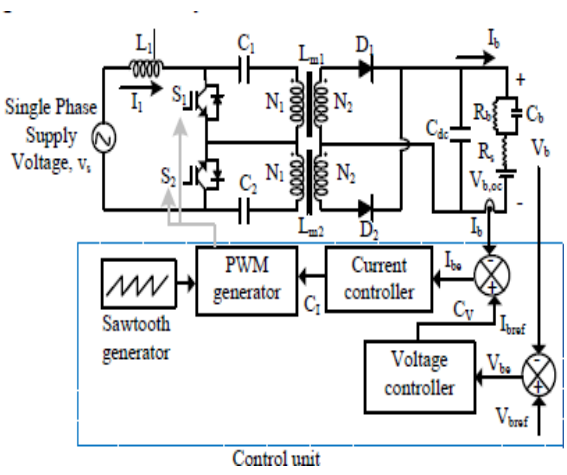

Fig. 2. Schematic of Bridgeless Isolated SEPIC PFC Converter used for battery charging

A unity power factor operation as well as improved load regulation is achieved with specifically designed components for the proposed converter and constant current/ constant voltage control mode of charging has to be implemented with the help of two PI (Proportional and Integral) controllers. The above mentioned controllers perform well to provide fast dynamic loop response and minimum steady state error to regulate DC link to the desired reference value so that a continuous current flows into the battery.(2)

III. MODES OF OPERATION

The principle of operation of the proposed bridgeless PFC converter to provide unity power factor operation as well as an input current free from any harmonics so that international standards are not violated. Two different subsections, namely, operation during a complete cycle of supply voltage and operation during a complete switching period has been shown in Fig. 3-7. Fig.8 shows the associated switching waveforms during both the subsections of converter's operation.

A. Operation during complete cycle of operation.

The proposed bridgeless topology uses two switches which are gated to operate one by one in alternate half cycle of AC mains voltage (i.e. positive and negative cycles respectively). During positive half cycle of supply voltage, switch S1 is turned ON which makes diode D1 forward biased as depicted by

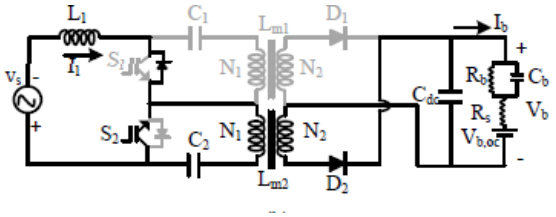

Fig. 3. MODE:1 During complete cycle of the supply voltage(positive half cycle)

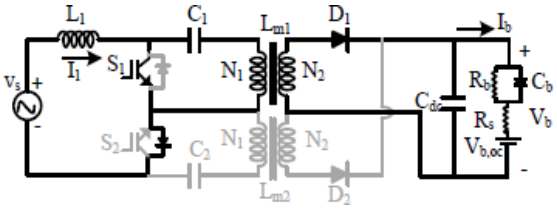

Fig. 4. MODE:2 During complete cycle of the supply voltage(negative half cycle)

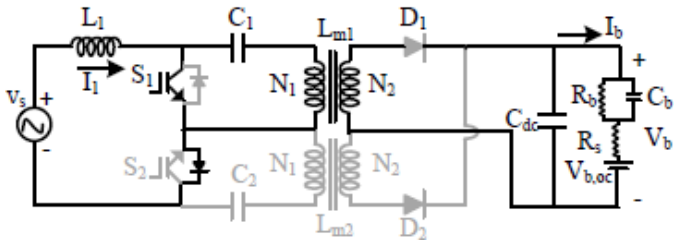

Fig. 5. MODE:3 operation during a complete switching period

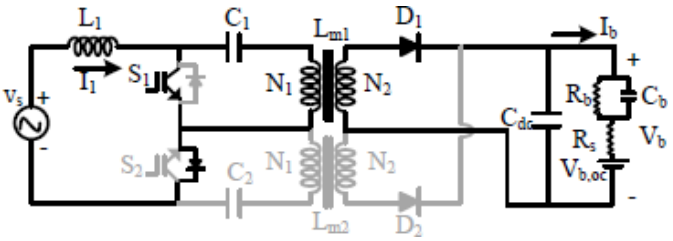

Fig. 6. MODE:4 operation during a complete switching period

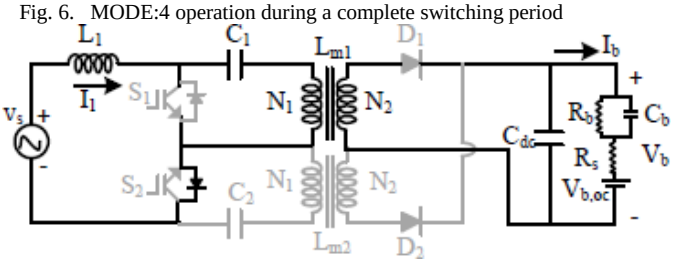

Fig. 7. MODE:5 operation during a complete switching period

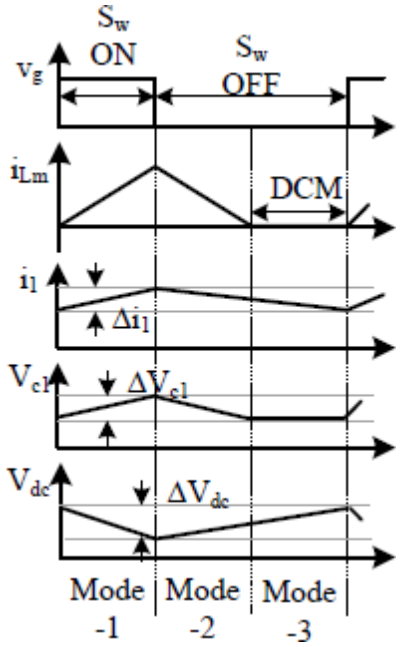

Fig. 8. Associated switching waveforms during positive or negative half cycle of the supply voltage. switch S2 remains OFF due to gating sequence generated by PWM control. After that, in negative half of the supply voltage, switchS2 and diode D2 come into conduction giving a reverse bias to diode D1 since switch S1 is in OFF condition, as depicted in Fig. 3(b).

IV. OPERATION DURING A COMPLETE SWITCHING PERIOD

The proposed circuit operates in three different modes as indicated in Figs. 2(c), (d) and (e) during positive (or negative) half of the supply cycle. During mode-1, when switch S1 is in conduction, diode D1remains OFF because of HFT polarity. In this duration, HFT inductance stores the energy supplied from the input source. The output capacitor feeds to the battery load, as shown in Fig.2 (c). When switch S1 comes into OFF state as indicated in Fig. 2(d), the energy in magnetizing inductance discharges through a diode D1 and it become forward biased, freewheels the HFT energy to the load. Fig. 2(e) shows the discontinuous operation of the proposed converter when a current in magnetizing inductance ceases and diode D1 again comes to OFF state. Similar

operation for the converter is seen for the negative half of the supply voltage, when switch S2 comes into conduction.

A. Design procedure of PFC circuits.

This section elaborates the design expression and control strategy used for charging along with representing Thevenin's equivalent model of lead acid battery. A 1kW PFC bridgeless SEPIC converter is designed for EV battery charging with the specifications given as: Output power (Pout) = 1kW, supply voltage (Vs) = 220V, DC link voltage (Vb) = 65V, line frequency (f) = 50 Hz, transformation ratio of HFT (N1:N2)= 1:1.015, permitted ripple current in inductor L1 (ΔiL1)= 50% of I1, permitted ripple voltage in intermediate capacitor C1(ΔVc1) = 25% of Vsav (average value of input voltage), (ΔVdc) permitted DC link voltage ripple = 10% of Vdc, switching frequency, fs= 50kHz. Battery rating: 48V 100Ah lead acid battery.

B. Design of Lead Acid Storage Battery

Fig. 3 shows a lead acid battery equivalent model, implemented in MATLAB/Simulink environment with the design parameters defined for the application.

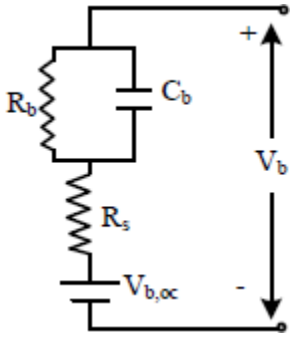

Fig. 9. Design of Lead acid storage battery

The Thevenin's equivalent circuit parameters are explained as a DC voltage source Vb, oc,, having a value of nominal battery voltage, an equivalent series resistance Rs of 0.01Ω that also includes internal resistance of battery, Rb, defined as self discharge resistance having value of (10kΩ) and an equivalent capacitor Cb which represents the storage capacity of the battery. The value of Cb for the battery storage capacity given in kWh is estimated as,

$$C_b = \frac{kwh*3600*1000}{0.5(V^2_{b,oc,max} - V^2_{b,c,\min})}$$

where,Vb,oc,max and Vb,oc,min are having the values of battery voltage in fully charged/discharged conditions i.e. 56V and 42V for a 48V 100Ah battery. Substituting the rated in (1), the estimated value of storage equivalent capacitor is obtained as

C. Design Procedure of Proposed Bridgeless PFC

1kW, 65V bridgeless PFC converter based EV battery charger with an isolated SEPIC converter topology is designed to operate in DICM depicted by discontinuous magnetizing inductor current in the end of each switching cycle. Various design expressions for different components of the proposed EV charger circuit are given here along with the design specifications chosen for the application. The operation of the proposed bridgeless SEPIC converter during both the halves of the supply is analyzed as below: The average value of input supply voltage, Vs is given by,

$$V_{sav} = \frac{2\sqrt{2}*V_s}{\pi} = \frac{2\sqrt{2}*220}{\pi} = 198V$$

Duty cycle for the application is considered as 0.25 in order to obtain 65V DC from rated 220V AC supply. Based on the value of the duty cycle, turns ratio of the HFT is being decided

$$V_b = \frac{(N_2/N_1)_{sav}D}{(1-D)}$$

Where, Vb is the specified DC link voltage at the output. Putting all the design value in above expression, HFT turns ratio N1/N2 comes out to be 1.015. The value of input inductor is given by

$$L_1 = \frac{V_s D}{2f_s \Delta i_1} = \frac{220 * 0.25}{2 * 50000 * 0.5 * (\frac{1000}{220})}$$

$$= 0.242mH$$

Where, fs is the switching frequency considered as 50kHz for the purpose. Substituting all the values in input inductor is estimated as 0.242mH for 50% ripple in input current

$$Where, K = \frac{2 * fs\ Leq}{R_b}$$

Here, Lm1 and Lm2 are given as HFT inductances gt /for the two isolated transformers and Ro is defining a battery load estimated as

$$R_o = \frac{b}{P_{out}} = \frac{65^2}{1000} = 4.225\Omega$$

The critical value of HFT inductance to operate under boundary conditions, is calculated as,

$$L_{mc} = (\frac{N_1}{N_2}) \frac{V_0(1-D)^2}{2Df_s I_0}$$

$$= (1.015)^2 \frac{65(1-0.25)^2}{2*0.25*50000*15.38} = 96.51\mu H$$

The value of Lm is selected as 30μHusing so that current through the inductor ceases at the end of each switching period.

The intermediate capacitors C1 and C2 are designed to operate in DCM consisting a ripple of 25% in intermediate capacitor voltage,

$$= \frac{V_b D(N_2/N_1)}{(\Delta V_{c1} f_s R_b} = \frac{65 * .025 ** 0.125}{0.25 * 198 * 50000 * 4.225}$$

$$= 1.52\mu F$$

Where, voltage across the intermediate capacitors is the average supply voltage due to DCM operation of the converter in steady state condition. A .08µF capacitor value is chosen to operate C1 and C2 into DCM. The DC link capacitor to supply rated battery load for 10% ripple in output voltage, is estimated as,

$$C_{dc} = \frac{I_b}{(2\omega\Delta_b}$$

Replacing the notations in (10), with the numerical values specified for the proposed converter, the value of the output capacitor is given as,

$$C_{dc} = \frac{I_b}{(2 * 314 * 0.1 * 65)} = 3.76mF$$

Therefore, a 4mF capacitor is selected to maintain the charging signals at specified levels and to control DC link voltage constant around 65V.

V. SIMULATION CIRCUIT

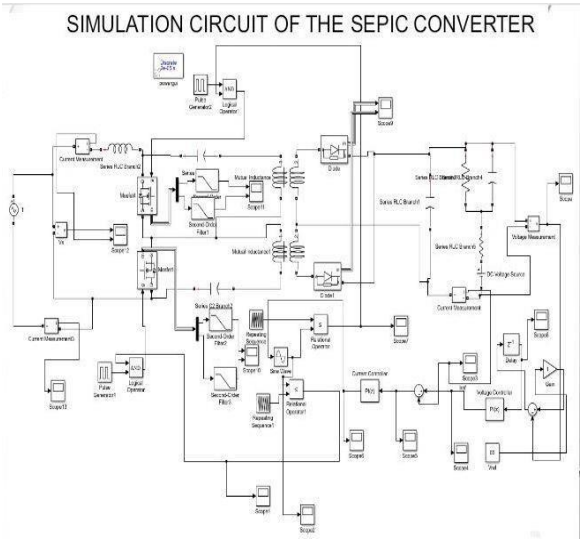

Fig. 10. Simulation circuit for SEPIC converter

We have propsed the a PFC bridgeless SEPIC converter used with the specified values. according to the standard specifications. we have got the waveforms that we have verified with the hardware.

The input voltage that we are giving in the simulation is 440(p-p).output that we are getting is at the battery side is 48v.a constant voltage.

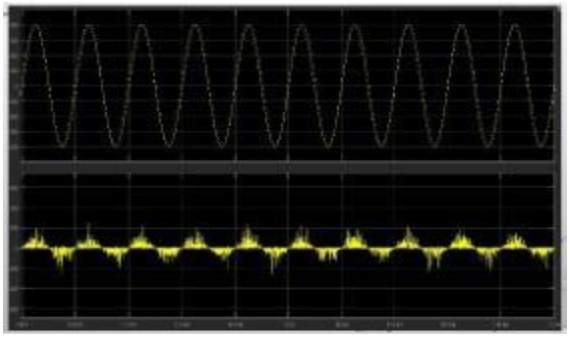

Fig. 11. INPUT VOLTAGE AND CURRENT400V(P-P)

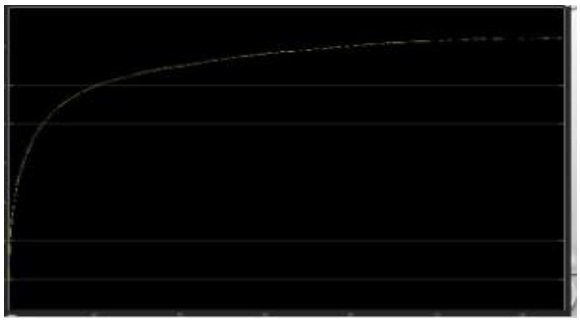

Fig. 12. Output Voltage48v(Constant)

VI. HARD WARE IMPLIMENTATION AND OUTCOME.

In hard ware we have used the same values as that of the simulation.ie at the input side we are giving 100v(p-p).and we have got the battery output 12v constant.

Fig. 13. Hardware circut

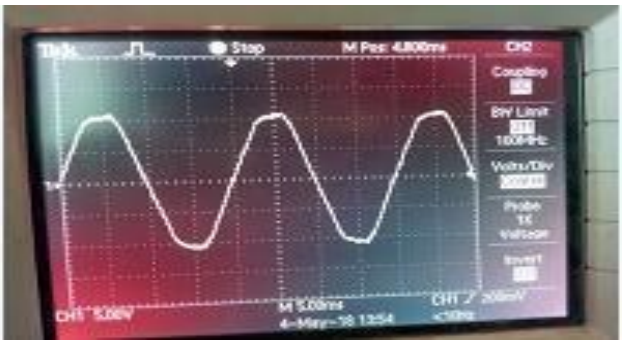

Fig. 14. 100v(P-P) Output Voltage

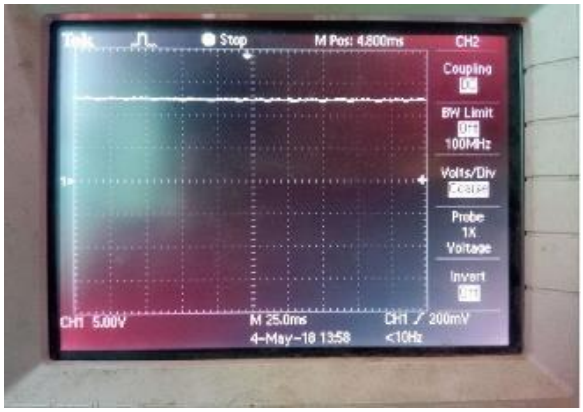

Fig. 15. 12v(constant battery output)

VII. CONCLUSION

Simulated results have implied the fact that proposed PFC converter is fast enough to reject any disturbances in the input AC mains voltage so that a constant charging current flows into the battery maintaining desired DC link voltage. In hard ware we have used 100v(p-p) & output that we are getting from the battery is 12v.In simulation we are giving 400v(p-p) & output that we are getting is 48v. The main intension is to make power factor to unity,& we have reduced the over all size of the components. We have compared the both simulation and hardware.and results is verified with the wave forms.

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