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A Comprehensive Study on implementation of Low Noise Amplifier

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***Abstract*-- A RF receiver design requires a Low noise amplifier that provides sensitivity to the system. The paper gives vast idea on designing low noise amplifier using different techniques. Low noise amplifier is the primary part of the receiver section of the system. The LNA provides an amplification of the collected weak signal to achieve minimum noise contribution. Applying CMOS technology in designing a low noise amplifier is the most preferred topics in the field of research as it is advantageous over low power, low cost and higher integration.**

Keywords--- LNA, CMOS technology, RF receiver, Noise Figure (NF), ULV, ULP, ULW.

I. INTRODUCTION

Nowadays, different standards are taking growth to provide applications on various fields at different frequency bands. A Low noise amplifier is the simple and foremost part used for designing a receiver. It amplifies the received weak signal and also reduces the noise and other distortion exist in the signal. Low Noise Amplifiers or LNA having trimming functions is introduced for designing microcircuits in CMOS technology. LNA plays the vital role in the millimetre- wave applications such as Earth science radiometry, passive remote sensing, radio astronomy and, transceivers.

LNA design provides the trade-off between linearity of the circuits, gain of amplifier, power dissipation, and also noise figure (NF) ratio. Low noise figure and high gain is the main requirement for the best working of a Low Noise Amplifier. To determine the efficiency of LNA it is necessary to analyse parameters like gain, noise figure, stability, and linearity in circuit. They convert the radio wave or electromagnetic wave which are exist in the surrounding, to give users with the proper information.

With higher advantageous factors like reducing of size, higher level of integrability, less manufacturing cost, etc., involved in designing the CMOS is a useful and combative technology for implementing radio transceiver. Many other methods have been used for designing Low Nosie Amplifier other than CMOS technology. CMOS technology is implemented because of the requirement of low production cost and higher transistor concentration. CMOS technology of 0.35µm, 0.18µm, and 0.13µm is widely used in designing Low Noise Amplifier with 0.13µm technology being an advanced technique used for its property of reduced chip size. Frequency ranges of cell phones, GPS, Bluetooth are covered. The aim of this paper is to give a keen opinion on using different techniques for designing Low Noise Amplifier.

Section II consists of a literature review of low noise amplifier designs and the Conclusion in sections III.

II. LITERATURE REVIEW

Different Low Noise Amplifier with various design techniques are listed below:

The paper [1] gives low-noise amplifier (LNA) designed using inductorless low power differential method which is designed in 65nm CMOS technology. The cross-coupled push-pull structure in LNA is used to achieve g_m boosting and partial noise cancelling under low power consumption, which depends on combination of CS stage and CG stage having shunt feedback topologies. To reduce the Miller-effect a cascode amplifier is used, which also creates a current steering structure to improve gain and bandwidth. This technique gives good results on establishing the overall performance trade-off after sizing and biasing optimization under the power constraint as these properties are required in the applications like wireless mobile devices and remote sensors to have an improved trade-off between power and performances [2]. On implementing this design of LNA, it provides 21.2dB of a voltage gain, and 2.8- 4dB of a noise figure.

The paper [3] describes the method for designing an ultra-low-power and ultra-low-voltage ultra-wideband feedback containing resistive-shunt LNA. Here, the fabrication is based on 90nm CMOS technology. In order to enhance the bandwidth and noise performance of the Low Noise Amplifier, the process involved analysis and usage of the feedback loop with the series inductive peaking. This designing technique makes use of a new biasing metric, and it also employs a current-reuse scheme. The extended ULP ULV biasing metric is defined as the product of the transconductance efficiency, intrinsic gain, and transit frequency as Biasing Metric ULP, ULV $=(g_m/I_D)\cdot(g_m/g_{ds})\cdot f_T$. The main objective of this paper is to find the optimum biasing point where the BW and gain are maximum and the NF is minimum while burning the lowest possible current. The result of measuring shows 12.6dB voltage gain, and the noise figure of 5.5dB.

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The paper [4] explains the trimming concept denotes that the frequency shift, can be compensated, which occurs due to process variations, model uncertainties, and underestimated parasitic components. In the non-trimmed state, this LNA showed a shift in gain towards lower frequencies. After trimming to 24GHz which is the specified operating frequency, only 0.3dB of a gain degradation is observed. As the active trimming in microwave circuits usually suffers heavily from lossy switches and varactors. Therefore, in this work, a trimming approach based on laser trimmable lumped elements is analysed for frequencies around 24GHz. The trimmed LNA achieves a peak gain of 20dB at 24GHz with a 3dB-bandwidth from 21 to 28GHz, a noise figure of 3.7dB, and an OIP3 of 15dBm. This LNA is provided with ESD protection and can work with a single voltage supply. The power consumption and the chip size are 17mW and 0.13mm^2. The 20dB gain and 3.7dB noise figure are required to widen the dynamic range and the application structure. It also contains a single-ended antenna for simplicity and cheaper integration cost.

The paper [5] discusses the process of designing a low-noise amplifiers (LNAs) for both room-temperature and cryogenic operation in general and takes the linearity and stability of the amplifiers into special consideration. Oscillations in the multi- finger transistor are studied and simulated and the measurements are reported. This design approach is used for designing LNAs for wideband receiver systems that require linearity and high gain from the RF-amplifier chain. This method of designing gives a practical view by making use of a three-stage LNA packaged in a WR10 waveguide casing and is fabricated by using 35nm InP HEMT technology that helps in achieving more than a 20dB gain from 75 to 116GHz and 26–33K noise temperature from 85 to 116GHz when cryogenically cooled to 27K.

A noise parameter and third order intermodulation product (IM3) expressions is presented in the paper [6] that provides input matching and power constrained noise at a same time for designing a low noise amplifier optimization technique. These expressions explain the methodology in designing a Low Noise Amplifier to record the power constrained noise and input matching and also satisfying the condition of linearity. A positive feedback is used to obtain a power gain. Here, fabrication is based on 0.18µm CMOS technology. This Low Noise Amplifier shows result with the power gain of 20dB and the Noise figure of 1.5dB.

In the paper [7], a low noise amplifier designed using feedback containing shunt resistive is introduced. Since most of the LNA makes use of series inductive feedback topology which provides more gain and good noise figure characteristics. But this topology faces certain drawbacks of producing the inductor value for the source degeneration which are crucial to impedance matching (Z_{opt} and Z_{in}). As a result, inductors are designed inside the IC's. This causes the degradation of noise figure on simulation. Hence shunt resistive feedback topology is used. This LNA, on implementing gives a gain of 12.4dB and a noise figure of 4.2dB.

In the paper [8], they have introduced two stages with the common emitter and cascode topologies in the first and second stage to achieve minimal noise figure and maximum gain. To investigate the performance of the Common-Emitter in relation to the NF, the mathematical analysis of the NF of the first stage is computed. In both stages of the LNA, the current mirror is used to bias the base of the transistor. Transmission lines are used in the circuit to reduce against a poor noise factor by reducing current utilization. The designed LNA realizes a gain of more than 17dB and a noise figure of less than 4.3dB at 61GHz.

The paper [9] provides an idea of designing a low power, high gain low noise amplifier (LNA) design that involves current re-use inductors and a complementary MOS structure. Forward body biasing technique is applied to the amplifying transistor to achieve the gain variability. The current re-use inductors at the drain of the CMOS structure helps to share the drain current between PMOS and NMOS. The width of amplifying transistor is chosen to give minimum noise figure and good input matching. The circuit was designed using 90nm CMOS process. The result showed that the gain obtained is 8.05dB with a low noise figure of 2.14dB. The supply voltage used in this LNA design is 1.1V resulting in a power consumption of 2.607mW.

The paper [10], the LNA is designed with 2- stage in which common source stage is followed by cascade stage. Here, the fabrication involves usage of 180nm CMOS technology. To obtain best results as well as minimum loss, different matching techniques are applied at the input, output and intermediate stages. The system used for designing and simulating LNA is Agilent Advance design system in a 180nm CMOS technology and the result which is being measured gives a voltage gain of 38dB, the noise figure of 1.867dB at 4GHz frequency which suites DBS application.

The paper [11] presented designing of CMOS LNA which is fabricated using 130nm CMOS technology. This LNA can be used in Bluetooth applications that operates at 2.4-2.5GHz band. This LNA has inductive degeneration topology that gives low noise and high gain. This LNA designing contains two amplifying stages with on-chip inductors and capacitors. The source involves a cascode amplifier topology with inductive degeneration. Advanced Design System (ADS) is the software used for simulation. The LNA designed, exhibits 20.343 dB gain and 1.98dB noise figure.

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The paper [12] describes a low-noise amplifier (LNA) design used for 60GHz low power wireless communication in 65nm CMOS technology. The LNA introduced here involves two stages, they are, an input stage and gain stage with former containing capacitive cross-coupling technique and latter making use of current-reuse techniques. The result on implementing this design gives a gain of 15dB and a noise figure of 4.7dB.

III. CONCLUSION

This paper exhibits the numerous techniques in which the LNA can be constructed. Low noise figure and high gain are the main parameters to determine the working ability of the LNA. The narrow band LNA is designed at a 4GHz frequency on 180nm CMOS technology has a high gain of 38dB and low noise figure of 1.867 which seems to be efficient when compared to all other techniques that are described in this paper. The LNA here is designed with two stages which is a common source stage followed by cascode stage since the cascode stage is widely used in mm- used to design Low Noise Amplifier using different CMOS technology giving a certain range of gain and noise figure which varies in applied methods.

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