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A Comprehensive Study of Dynamic Power Management

Prateek Bindra
Assistant Professor, GEC, Panipat
prateekbindra@gmail.com

Abstract: Dynamic Power management (DPM) refers to the problem of judicious application of various low power techniques based on runtime conditions in an embedded system to minimize the total energy consumption.DPM uses a set of techniques that achieves energy-efficient computation by selectively turning off system components when they are idle (or partially unexploited). In this paper, we survey several approaches to system-level dynamic power management.

Keywords: - Dynamic voltage scaling, dynamic frequency scaling, break even time.

I. INTRODUCTION

This paper has the objective to cover and relate different approaches to system-level DPM. We begin by describing how systems are affected by changing the values of operating voltage and frequency and how the use of their dynamic reconfiguration can impact the overall power consumption. Next, we review and compare different approaches to DPM.
Three classes of power management policies have been proposed in the past: time-out, predictive, and stochastic policies [1], [8]. The fixed time-out policy shuts down the system after a fixed amount of idle time. Adaptive time-out policies are more efficient because they change the time-out according to the previous history. In contrast with time-out policies, predictive techniques do not wait for a time-out to expire, but shut down the system as soon as it becomes idle if they predict that the idle time will be long enough to amortize the cost of shutting down. A stochastic approach provides a polynomial-time exact solution for the search of optimal power management policies under performance constraints.

II. VOLTAGE SCALING

This section introduces the basic principles of power consumption and the effects of voltage scaling [2]. CMOS circuits have both dynamic and static power consumption. Static power consumption is caused by bias and leakage currents but is insignificant in most designs that consume more than 1 mW.

The dominant power consumption for CMOS microprocessors is the dynamic component. Every transition of a digital circuit consumes power, because every charge and subsequent discharge of the digital circuit's capacitance drains power. The dynamic power consumption is equal to

$$P = C f V_{dd}^2 \quad (1)$$

Where f is the number of clock cycles per sample period. *C* is the averaged switched capacitance per clock period and V_{dd} is the supply voltage It is clear from Equation (1) that reduction of V_{dd} is the most effective mean to lower the power consumption. Lowering V_{dd}, however, creates the problem of increased circuit delay. An estimation of circuit delay is given by

$$T_d = (C_L . V_{dd}) / k (V_{dd} - V_t)^2 \quad (2)$$

where, Td is the delay, V_{dd} is the supply voltage, C_L is the total node capacitance, k is process constant, V_t is the threshold voltage, The propagation delay restricts the clock frequency in a microprocessor. From Equations (1) and (2), it follows that there is a fundamental trade-off between switching speed and supply voltage. Processors can operate at a lower supply voltage, but only if the clock frequency is reduced to tolerate the increased propagation delay.

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The critical path of a processor is the longest path a signal can travel. The implicit constraint is that the propagation delay of the critical path T_d must be smaller than 1/f. In fact, the processor ceases to function when V_{dd} is lowered and the propagation delay becomes too large to satisfy internal timings at frequency f.

III. RELATED WORKS

3.1 Dynamic Voltage Scaling (DVS)

For studying DVS, various algorithms are applied to various processors and power management is analyzed. Various strategies used for dynamic power management are summarized here.

a) Adaptive Dynamic Power Management

An adaptive DPM strategy is based on the exponential-average algorithm. The algorithm applies the last time predicted idle period and the actual one as weighting factors. The weighting for each older data point decreases exponentially, giving much more importance to recent observations while still not discarding older observations entirely [3].

This model consists of two parts: DPM Predictor and DPM Controller. DPM Predictor implements the proposed adaptive prediction strategy which can be divided into three modules: Counter, Basic Predictor and Adjuster. Counter is deployed to record T_n, which stands for the length of last actual idle period. The Counter starts counting immediately after the processor enters into the idle status and stops counting when detecting a processor interruption. Then, the value of T_n is sent simultaneously to the Basic Predictor and the Adjuster. When Adjuster receives the new value of T_n, it calculates the adjusting factor *a*. Since the calculation of *a* need two previous idle time value, the Adjuster conserves data using a simple FIFO with depth of 2. When the new value comes in, the old one is discarded. During a DPM process using Longtium DSP core processor, lowering the clock rate of a processor affects only dynamic power and reduction in dynamic power is in the range of 10-27%.

b) Predictive DVS

Dynamic Voltage Scaling (DVS) is the scheduling algorithm that changes the operating clock frequency of the processor according to the supplied voltage. DVS algorithm, applied only to the tasks with lower priority. Process usage is derived by the idle task which has the lowest priority in the system [4].

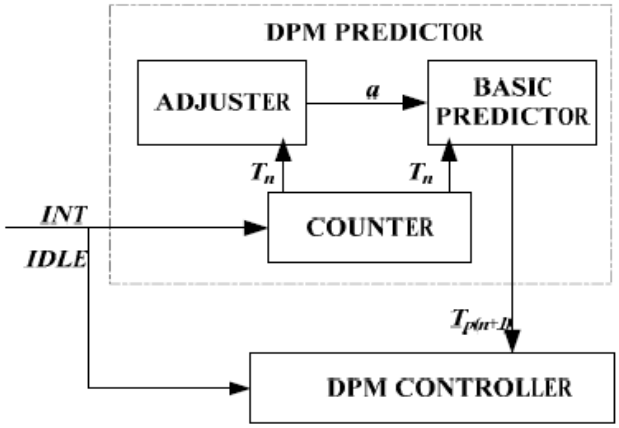

Fig 1: Adaptive DPM model [3]

Process usage indicates 0% if system executes idle task only because there are no tasks whose state are 'ready'. In a contrary concept, process usage will be 100% if idle task is not executed because there are lots of tasks whose state is 'ready'. Process usage (PU) is derived by this formula below:

PU = 100(1- (Idle TaskCount / TotalCount)) (3)

DVS is applied only when the process usage is higher than certain predefined value. As process usage increase, the amount of power consumption will decrease, but the probability of task with low priority being processed abnormally will increase.

c) Profile based DVS

Dynamic power management is done by analyzing profile based power consumption using control flow graph (CFG).CFG has I/O-access blocks at various arbitrary locations and it tells about the possible flows of execution for a program[5],[6]. This approach attempts to utilize the control flow profile of an embedded code to take power management decisions of the peripherals rather than the CPU, with due consideration given to both performance and power.

Two major concepts discussed are: Application model-CFG contains nodes of CPU related operations and peripheral (I/O) related operations.

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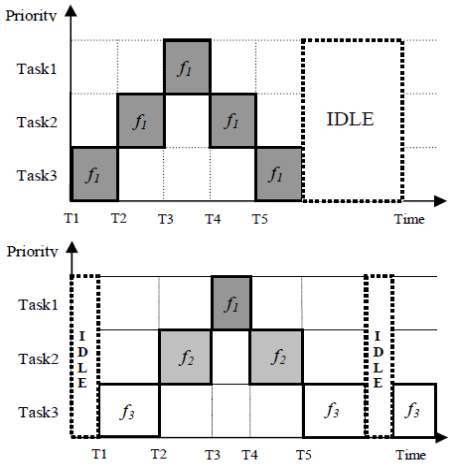

Fig 2: Predictive Scheduling for DVS [4]

Break even time-The minimum length of an idle period to save power is called the breakeven time (T_{BE}).

$$T_{BE} = T_{OFF} + T_{MS} + T_{ON} \quad (4)$$

Where T_{OFF}: Device turns off time, T_{ON}: Device turns on time, T_{MS}: Minimum sleeping time

An offline algorithm has been devised to decide about the dynamic power down of peripherals during their idle times for power management. The algorithm consists of two steps: Identifying appropriate Switch-ON points ensuring performance and identifying profitable Switch-OFF points for energy saving. To turn it ON, a Switch-ON point is placed along every path which leads to that I/O block at a location in the CFG which has "enough time" (i.e. T_{ON}) to Turn-ON the peripheral without performance penalty. This ensures that the device will be turned ON along all possible entries of an I/O access. Among all possible paths from one I/O access to the successive I/O access, if the shortest path has profitable time ($>T_{BE}$) to Turn-OFF the peripheral without power penalty, then a Switch-OFF point is placed along every path from the current I/O block to the next I/O block. With this proposed method, the worst-case potential idle time duration for energy savings depends upon the shortest time duration taken by a Switch OFF point to meet the nearest Switch ON point. Hence, the energy savings is much dependent upon the density of I/O access blocks. Less closer they are, more opportunities for energy savings. Hence an application with relatively larger distances among consecutive I/O access blocks along several paths of execution can gain much from this approach.

3.2 Dynamic Voltage Frequency Scaling

In this approach the energy consumption is reduced by changing dynamically the supply voltage and operating frequency. One of the techniques used is discussed below.

a) Deterministic Stretch-to-Fit (DSF)

It is based on the slowdown strategy of reducing the processor power consumption [7]. Slowdown is known to reduce the dynamic power consumption at the cost of increased execution time for a given computation task. It detects early completion of tasks and exploits the processor resources to reduce the energy consumption. In Fig 3, by comparing the actual execution time (AET) of a task $T1$ with its worst-case execution time $WCET$) $C1$, (DSF) technique determines the value of the dynamic slack (ϵ). This slack time is exploited by the method to reduce the energy consumed, by stretching the execution of $T2$, having $C2$ as WCET, and reducing the frequency of the processor. $tdisp$ is the available time at current processor frequency f. $t1$ and $t2$ represent respectively the activation date of $T1$ and $T2$.

IV. RESULTS AND DISCUSSION

Various kinds of processors are used to study DPM using above discussed techniques. For DVS, SA-1100 processor is used to analyze the voltage and frequency scaling effect on the power consumption of the system in which frequency can be varied from 59 MHz to 251MHz. Supply voltage can be varied from 0.8 V to 2.0 V. To see the application performance, H.263 decoder is used and power consumption is measured with respect to the clock frequency. Power consumption is studied for two modes: idle and cpu - intensive. At the lowest clock frequency the processor consumes 1/5 of the energy per instruction that is required at peak performance. Numerical values: At 59 MHz: 105.8 mW and at 251 MHz: 963.7 mW is consumed. The frequency and voltage can be scaled dynamically from user space in only 140 us. This allows pow er-aw are applications to quickly adjust the performance level of the processor whenever the workload changes.

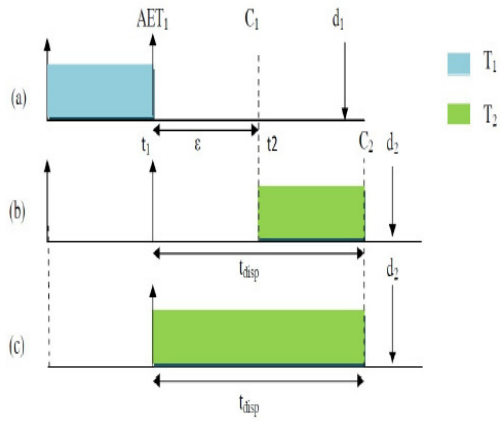

Fig 3: Slack reclamation using the DSF technique [7]

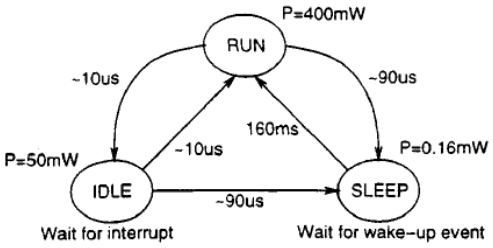

Fig 4:Power state transition of SA-1100 processor [9]

For DVFS, the target hardware platform is the OMAP35x EVM board from MISTRAL (TEXAS INSTRUMENTS). It is equipped with the OMAP 3530 processor, an advanced superscalar ARM Cortex-A8 RISC Core. The models of the context switch energy consumption are integrated at a system level, the context switch consumes 6% of the energy consumed by the application.

V. CONCLUSION

We surveyed several classes of power-managed systems and power management policies. Furthermore, we analyzed the tradeoffs involved in designing and implementing power-managed systems. Several practical examples of power-managed systems were analyzed and discussed in detail. Even though DPM has been successfully employed in many real-life systems, much work is required for achieving a deep understanding on how to design systems that can be optimally power managed.

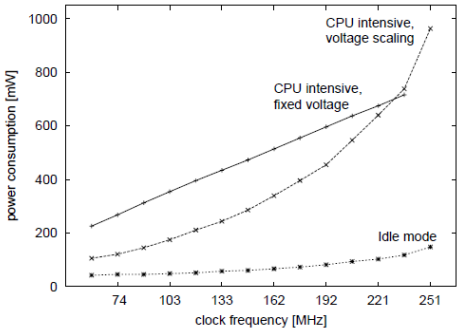

Fig 5: Total power consumption for idle and cpu -intensive workloads [1]

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