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A Comparision of Control Algorithms for DSTATCOM for Compensating Voltage Sag and Swell

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***Abstract*— In this paper, a 3-phase VSC-based DSTATCOM is implemented using the Backpropagation control algorithm and SRF theory for controlling power quality disturbances such as voltage sag and voltage swell. A control algorithm is employed to derive reference source current signals from the load current to get the switching pulses for IGBTs of the VSC of the DSTATCOM. Back Propagation (BP) control algorithm is predicated on the extraction of the elemental weighted value of active and reactive power components of load currents which are required for the estimation of reference source current and SRF theory is based on the transformation of currents in synchronously rotating dq frame. Back Propagation Control Algorithm and SRF theory-based DSTATCOM are simulated with MATLAB using SIMULINK for different types of linear loads. The performance of DSTATCOM is studied with proposed control algorithms for different types of loads. This electronic document is a "live" template and already defines the components of your paper [title, text, heads, etc.] in its style sheet.**

Keywords*— *DSTATCOM, Backpropagation (BP) control algorithm, SRF theory, Voltage sag, voltage swell, reactive power compensation, power quality, MATLAB/SIMULINK

I. INTRODUCTION

In modern distribution systems, the major power consumption is by reactive loads, such as fans, pumps, etc. The lagging power factor caused by these reactive loads increases the demand for reactive power in a distribution system. Excessive reactive power demand increases losses and reduces the active power flow capability of the distribution system [1]. Voltage sags and voltage swell are the most occurring power quality problems. And these problems are very common in heavy-loaded industries and they cause significant financial losses [2].

The FACTS technology opens new opportunities for enhancing the power capacity of the present, as well as new and upgraded lines. Load balancing, harmonic current mitigation, and reactive power compensation are major problems of AC distribution networks and a DTSATCOM is a solution to the above problems [3]. DSTATCOM is a shunt connected to the power distribution network. In addition to the above-stated problems, DSTATCOM also provides solutions to power factor corrections [4]. The major advantages of DSTATCOM compared with static VAR compensator (SVC) include the ability to generate the rated current at any network voltage, better dynamic response, and use of a relatively small capacitor on the DC bus side.

The current components are extracted from reference source current components. A control algorithm of DSTATCOM is used for this extraction. And thus it is crucial for a DSTATCOM. Instantaneous reactive power theory, Synchronous reference frame theory, Adaline-based neural network, and Back Propagation control are some of these control techniques [5]. The performance of a DSTATCOM is explored through design and simulation in this study. The back Propagation control method and SRF theory are utilized for the control of a DSTATCOM.

Section II presents the system configuration, mathematical formulations, and control algorithms used for the simulation model. Then section III presents results and discussions. Finally, in the last section, section IV conclusions are provided.

II. SYSTEM CONFIGURATION AND MATHEMATICAL FORMULATION

A. System configuration

A voltage source converter (VSC)-based DSTATCOM is connected to a three-phase AC Source with internal impedance feeding three-phase linear loads which are shown in Fig.1.For reducing ripple in compensating currents, the interfacing inductors (Lf) are connected at the ac output of the VSC. For proper PWM management of DSTATCOM's VSC, the DC bus voltage (Vdc) is determined by the Point of Common Coupling (PCC) voltage and must be larger than the amplitude of the AC mains voltage. The voltage and current rating of the required compensation decide the rating of the switches [6].

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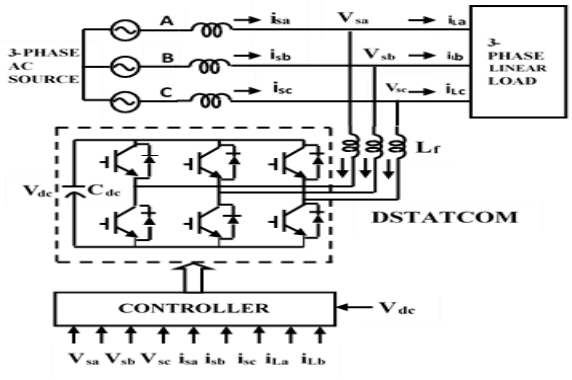

Fig. 1. Schematic diagram of VSC-based DSTATCOM

The selection of the DC bus voltage, DC bus capacitor, and AC inductors is based on the rating of DSTATCOM. The required values of DC bus voltage, DC bus capacitor, and AC inductor are obtained and given below.

A.1.1. DC Capacitor Voltage

For proper PWM management of DSTATCOM's VSC, the DC bus voltage (V_{dc}) is determined by the PCC voltage and must be larger than the amplitude of the AC mains voltage. The voltage of the DC bus (V_{dc})is given as,

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{m*\sqrt{3}} \qquad (1)$$

Where m = modulation index and is considered as 1

V_{LL}= AC line output voltage of DSTATCOM

A.1.2 DC Bus Capacitor

The DC Bus Capacitor is given by equation 2.

$$C_{dc} = \frac{(\frac{X}{2}+2X)*NOOFCYCLES*TIMEPERIOOCYCLE}{(1.8V_M)^2-(1.4V_M)^2} \qquad (2)$$

Where X = rating of the converter and V_M = peak value of phase voltage

A.1.3. AC Inductor

The selection of the AC inductance depends on the ripple current, $i_{cr,}$ and switching frequency F_s, The AC inductance is given as

$$L = \frac{V_{dc}}{4*h*F_{smax}}$$

$$h = \sqrt{\frac{K_1}{K_2}} * \frac{2(m^2-1)F_{smax}}{4m^2}$$

$$m = \frac{1}{\sqrt{1-\frac{Fsmax}{Fsmin}}} \qquad (3)$$

Where F_{smax} and F_{smin} is maximum and minimum switching frequency, K_1, K_2 are constants.

B. Control Algorithms

The control algorithm is used for the extraction of reference source current components. In this paper, the Backpropagation (BP) control algorithm and SRF theory are used to extract reference source currents components

B.1.1 Back-Propagation (BP) Control Algorithm

The Back Propagation training process is shown in Figure 2, as a block diagram for estimating reference source currents using the weighted value of load active and reactive power current components. [3]. In this BP algorithm, the phase PCC voltages (Vsa, Vsb, and Vsc), source currents (isa, isb, and isc), load currents (iLa, iLb, and iLc), and dc bus voltage (Vdc) is required for the extraction of reference source currents (isa*, isb* and isc*). There are two primary modes for the operation of this algorithm: The first one is a feed-forward, and the second is the Back Propagation of error or supervised learning[7]of the current designations.

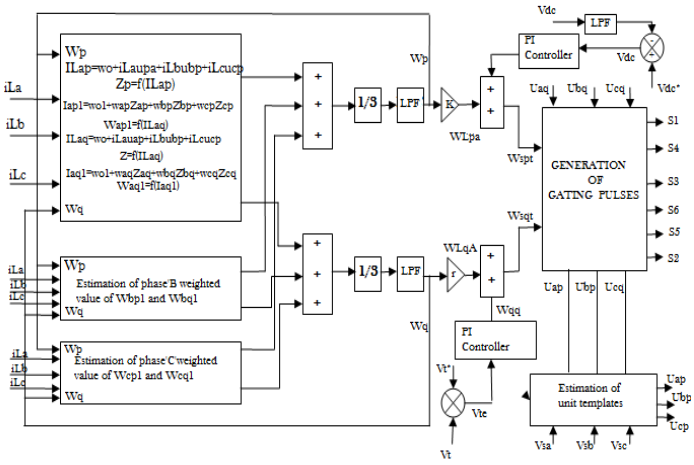

Fig.2 Block diagram of the reference current extraction using Back Propagation control algorithm

B.1.2 Synchronous Reference Frame (SRF) Theory control algorithm

Another most commonly used control algorithm method is the synchronous reference frame control algorithm (SRF). This algorithm is based on the transformation of currents in a synchronously rotating dq reference frame. Fig.3 shows the block diagram of SRF theory. Input signals V_{sa}, V_{sb} and V_{sc} and i_{La}, i_{Lb}, and i_{Lc} are sensed and fed to the controller. To produce unit voltage templates, voltage signals are applied to a phase-locked loop (PLL) (sine and cosine signals). Current signals are transformed to a dq reference frame, where these signals are filtered and transformed back to abc frame (i_{sa}, i_{sb}, and i_{sc}), which are fed to a sinusoidal PWM signal generator to generate gating pulses for switches of the DSTATCOM.

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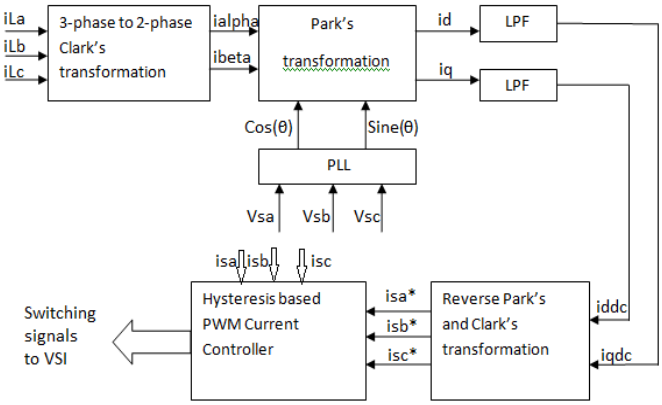

Fig.3 Block diagram of the control algorithm using Synchronous Reference Frame Method

III. RESULTS AND DISCUSSION

The main components of the simulation model are of a control block, source, DSTATCOM, and load. The data used in the simulation model is given below. AC supply source: three-phase line voltage, 415 V, 50 Hz, Source impedance: R_S = 0.04 Ω and L_S= 2 mH, Load 1: R Load (10KVA), Load 2: RL Load (3KW, 50KVAR), Load 3: RL Load (3KW, 50KVAR), Rating of VSC = 60 kVAR, Switching frequency of inverter = 10 kHz, Reference dc bus voltage: 700 V, DC bus Capacitance(Cdc)=8000µf , Interfacing inductor ($L_{f)}$ = 2.75 mH, Gains of PI controller for dc bus voltage: k_{pd} = 3.6 and k_{id}=0.9, Gains of voltage PI controller: k_{pd}= 2.55 and k_{id} = 4, Selected initial weights: W_0 = 0.4 and W_{01} = 0.2
Learning rate (μ) = 0.6, Cut off frequency of low-pass filter used in dc bus voltage = 15 Hz, Cut off frequency of low-pass filter used in ac bus voltage = 10 Hz, Weights of hidden layer for Back propagation control algorithm For ZVR MODE: $W_{ap}=W_{bp}=W_{cp}=0.4$, $W_{aq}=W_{bq}=W_{cq}=0.6$, For PFC MODE: $W_{ap}=W_{bp}=W_{cp}=0.4$.

Simulation is carried out in discrete mode at a maximum step size of 2.5 ×10-6s. A lagging load connected to a three-phase system absorbs reactive power from the system and causes a dip in PCC voltage called voltage sag. The main objective of the control is to maintain the PCC voltage at a nominal value by controlling the fluctuation in the voltage. The Simulink model for this system is shown in Fig.4

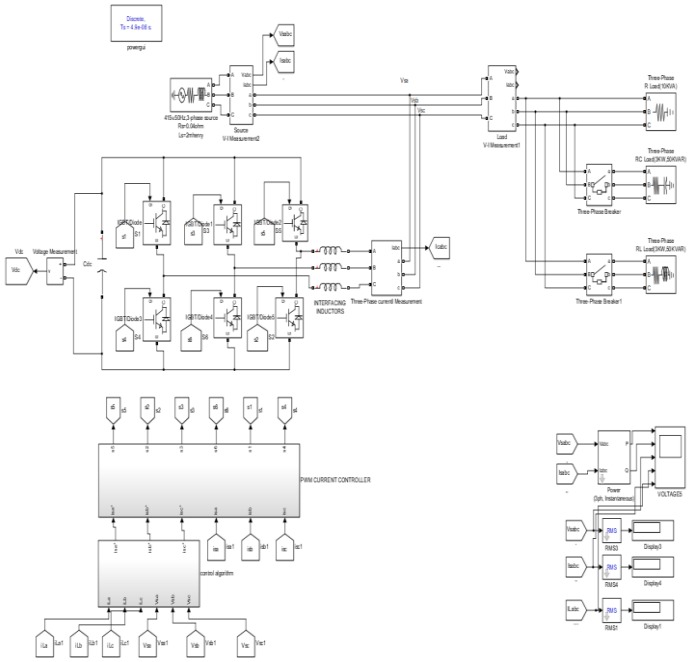

Fig.4. Simulink model of DSTATCOM using Back Propagation control algorithm

A. *Without DSTATCOM*

In the first stage, the system is simulated without connecting the DSTATCOM. At t=0sec circuit breaker1(CB1) and circuit breaker2(CB2), both are kept open connecting only resistive load(load1) to the system. The source current, the voltage measured at PCC, and load currents are 13.87amps,238.9volts, and 13.87amps respectively. When CB1 is closed at t=0.2sec. The source current, the voltage at PCC, and load current are increased to 87.6amps,291.9volts, and 87.6amps respectively due to the supplied Q power by the sudden addition of RC load(Load 2). At t=0.4sec, CB1 is opened and at t=0.5sec, RL load is connected to the system by closing CB2. In consequence, the PCC voltage is reduced to 202 volts, and the source current and load current are increased to 67.8amps. Reactive power Q is drawn from the system due to the sudden addition of RL load (Load 3). Simulation results for voltage sag and swell are shown in Fig.5

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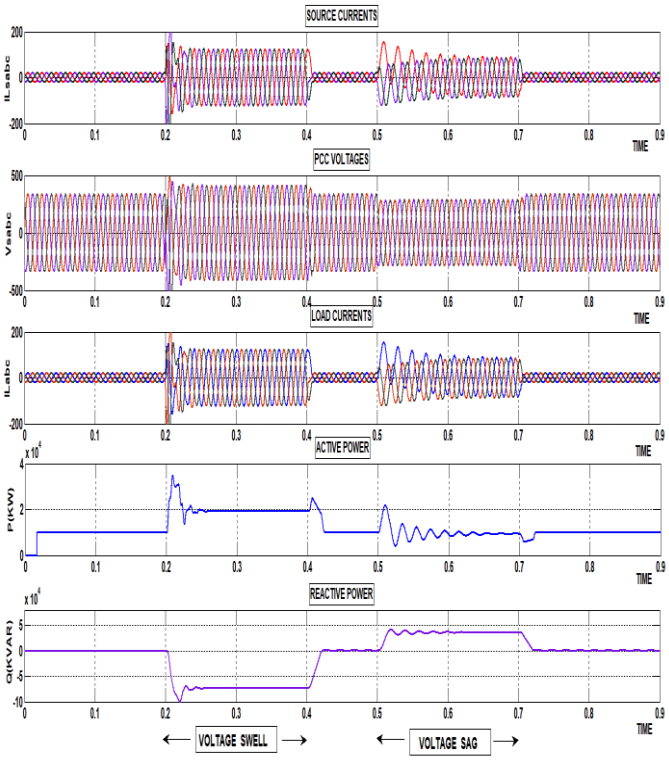

Fig.5 Output waveforms of R and RC, RL loads without DSTATCOM (a)Source current (b)PCC voltage (c)load current (d) Active power (e)Reactive power

B. With DSTATCOM

Now the DSTATCOM is connected as shown in Fig.4. This DSTATCOM is simulated with above mentioned Back Propagation Control Algorithm and SRF theory.

B.1.1 Back Propagation Control Algorithm

For RL and RC load conditions, the backpropagation algorithm of three-phase DSTATCOM under two modes of operations, namely, PFC and ZVR is studied.

B.1.1.1 Back Propagation Control Algorithm (ZVR MODE)

In the case of ZVR mode, regulation of PCC voltage is ensured by absorbing or injecting the required amount of reactive power.

The desired weighted values are assigned to the hidden layer and the average amplitude of the fundamental active and reactive power components are obtained, which are used to calculate the reference source currents.Fig.6 shows a simulation model of the backpropagation algorithm for ZVR mode.

These generated pulses are given to their respective switches for the switching of DSTATCOM for the compensation. Compensating currents are supplied by the DSTATCOM for reactive power compensation. Fig 7. shows the PWM control circuit used in the backpropagation algorithm.

The outputs of the Simulink model are shown in Figures 8,9 and 10. Fig.8 depicts DSTATCOM's DC link Voltage. In this case, DC link voltage is maintained at 700V. Fig.9 depicts the PCC Voltage. which is maintained at 340V (equal to the supply voltage). Fig.10 shows the PCC voltage, load currents, and source currents.

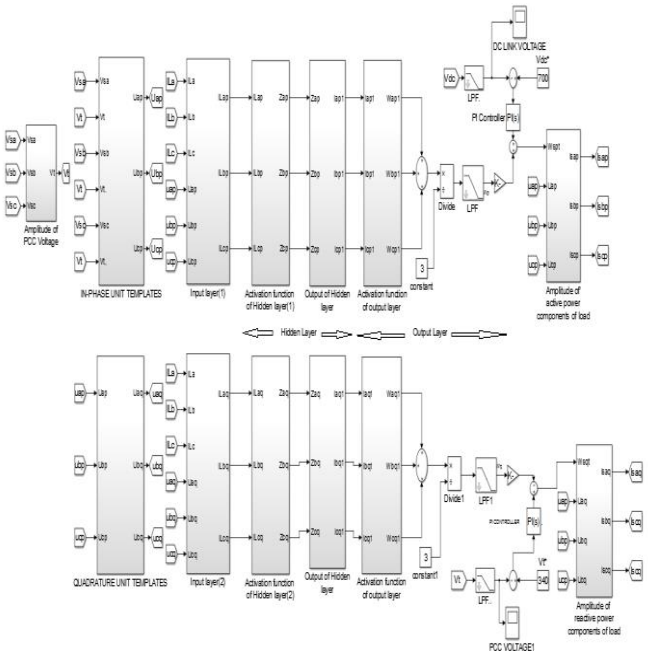

Fig 6 Simulation model of a Backpropagation control algorithm for ZVR mode

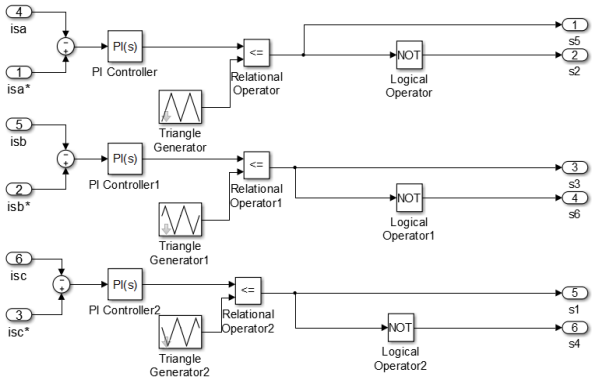

Fig.7 PWM control circuit

As shown in Fig.10 from t=0.2sec to t=0.4sec i.e during RC load, Source current, PCC voltage, and load current are 18.13amps,239.5volts, and 18.13amps respectively with the Backpropagation control algorithm when compared to 87.6amps,291.9volts, and 87.6amps without DSTATCOM and from t=0.5sec to t=0.7sec i.e during RL LOAD Source current, PCC voltage, load current are 18amps, 237.8volts and 18amps respectively when compared to 67.8amps, 202volts and 67.8amps without DSTATCOM. When loads are introduced at t=0.2sec and t=0.5sec, DSTATCOM either supplies or absorbs the reactive power and regulates the PCC voltage to a specific value

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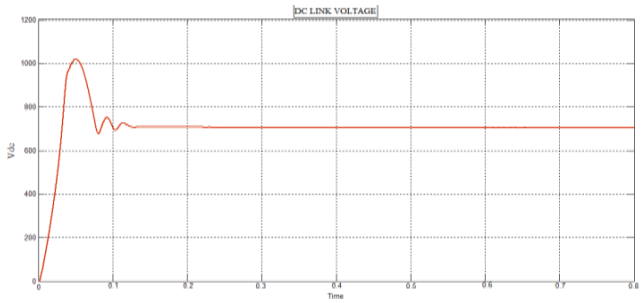

Fig.8 DC-Link voltage (ZVR mode)

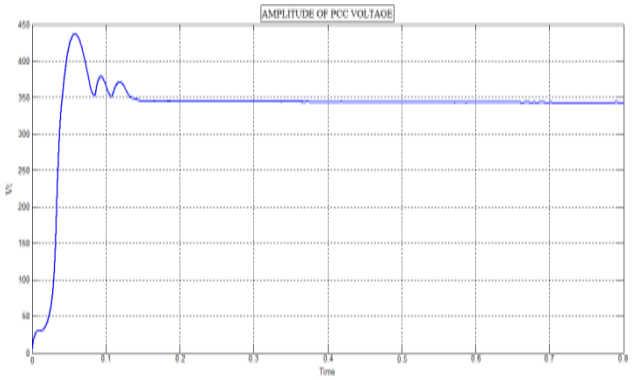

Fig.9 Amplitude of PCC Voltage(ZVR MODE)

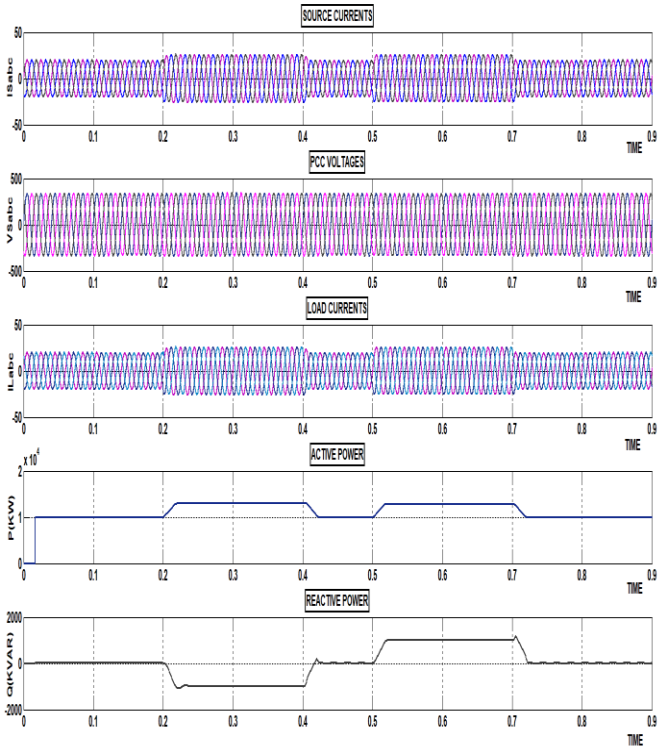

Fig.10. Output waveforms with DSTATCOM(ZVR mode)

(a) Source current, (b)PCC voltages, (c)Load currents(d)Active power(d)Reactive power

B.1.1.2 Back Propagation Control Algorithm (PFC MODE)

The performance of the BP algorithm for the three-phase DSTATCOM is studied for the PFC mode of operation under different load conditions. Fig 11. Shows the simulation model of a Backpropagation control algorithm for PFC mode.

Figures 12 and 13 illustrate the results of the Simulink model. The PCC voltage, load currents, and source currents are shown in Fig.12. DSTATCOM's DC link voltage is shown in Fig.13. The DC connection voltage is kept at 700V here.

From t=0.2sec to t=0.4sec, i.e. during the RC load, as seen in Fig.12, With the Backpropagation control algorithm, source current, PCC voltage, and load current are 19.65amps, 243volts, and 19.65amps, respectively, compared to 87.6amps, 291.9volts, and 87.6amps without DSTATCOM. During the RL Load, from t=0.5sec to t=0.7sec, the source current, PCC voltage, and load current are 18.95amps, 234.4volts, and 18.95amps, respectively, compared to 67.8amps, 202volts, and 67.8amps without DSTATCOM. DSTATCOM either supplies or absorbs reactive power and adjusts the PCC when loads are added at t=0.2sec and t=0.5sec.

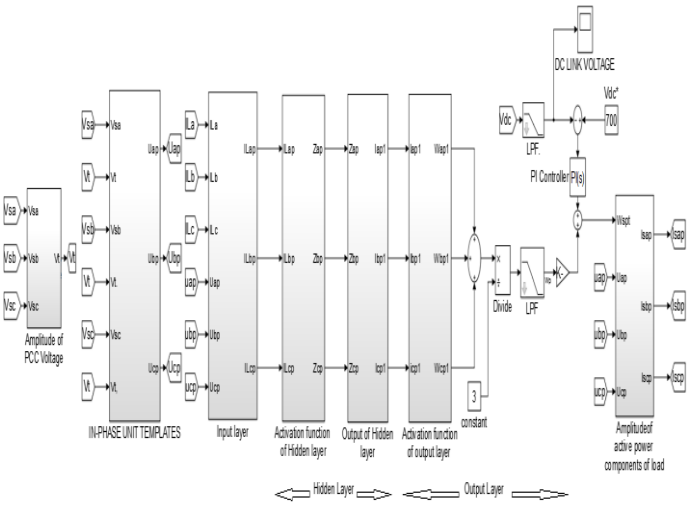

Fig.11 Simulation model of a Backpropagation control algorithm for PFC mode

B.2.1 Synchronous Reference Frame (SRF)Theory

The simulation model of the control block using SRF is shown in Fig.14. The simulation is run for a total time duration of 4 sec. The load voltages are used for the calculation of unit templates with the help of a Phase-locked loop (PLL).

With the help of unit templates, the load currents are transformed into two-phase coordinates using Park's transformation i.e., DQ coordinates. The transformed currents are as shown in Fig 15.

As seen in Fig.15, the currents contain both mean and oscillating components. Here we require only the mean or dc component of currents for the generation of reference source currents. The DC component of powers is extracted using low

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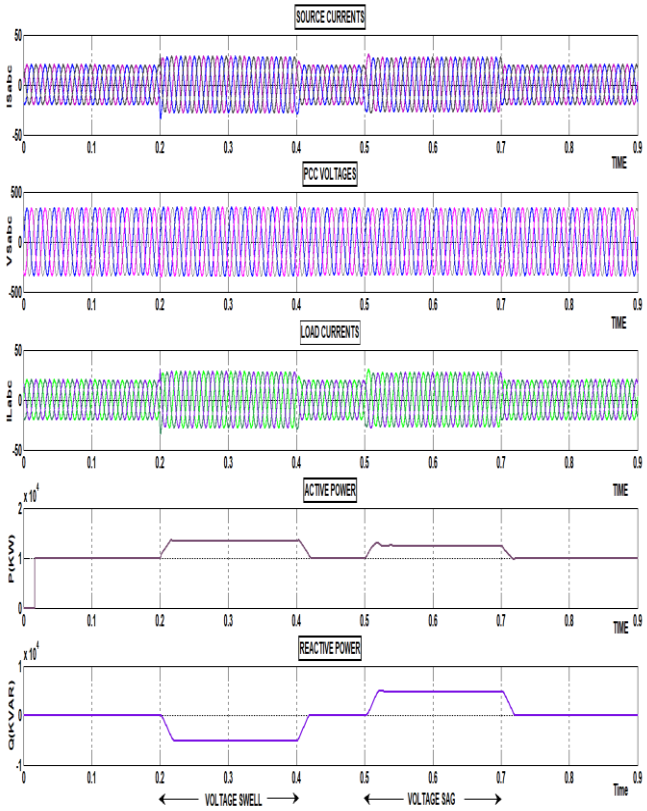


Fig.12 Output waveforms with DSTATCOM(PFC mode) (a)source current(b)PCC voltage(c)Load currents (d)Active power (e)Reactive power

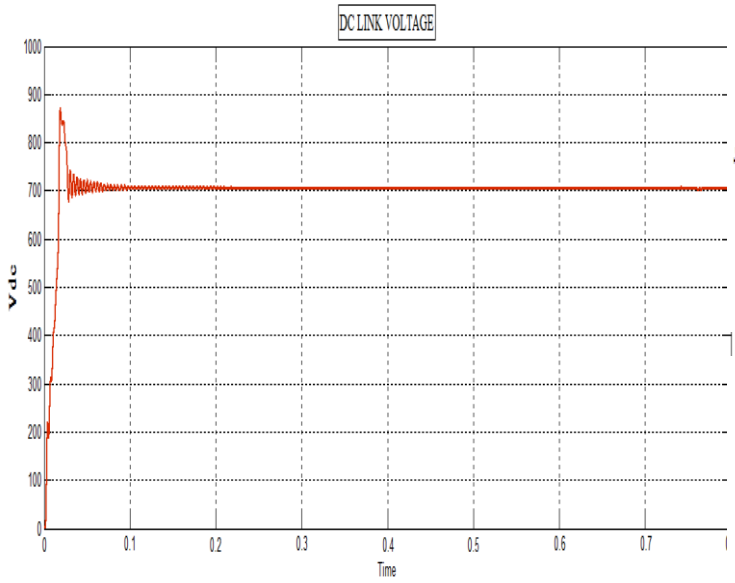


Fig.13 DC-Link voltage (PFC MODE)

pass filters. The currents after filtering are as shown in below Fig.16.

The second order Butterworth filter is used for extraction of the DC component of i_d and i_q currents. These DC components of currents are transformed into three-phase coordinates using reverse parks and reverse Clark transformation.

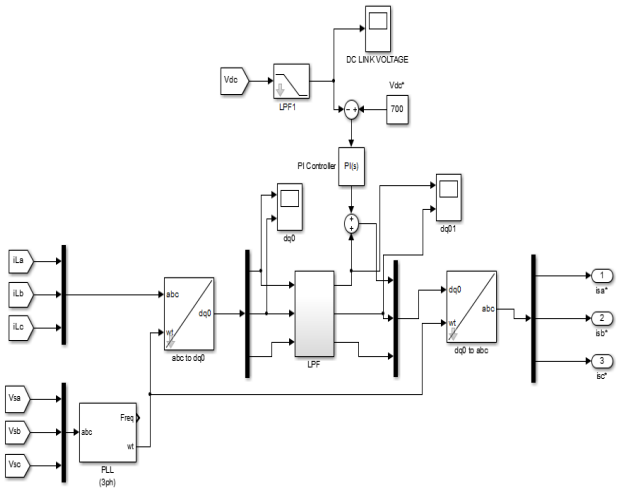
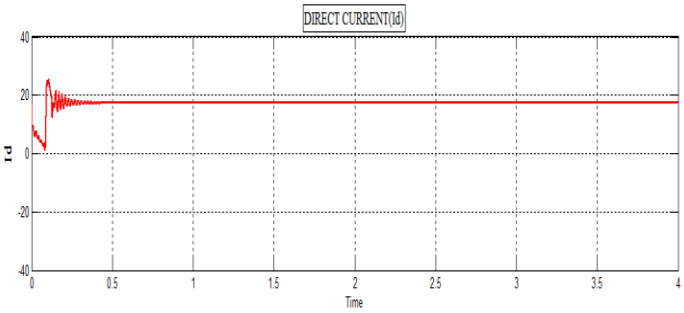


Fig.14 Control blocks using SRF theory



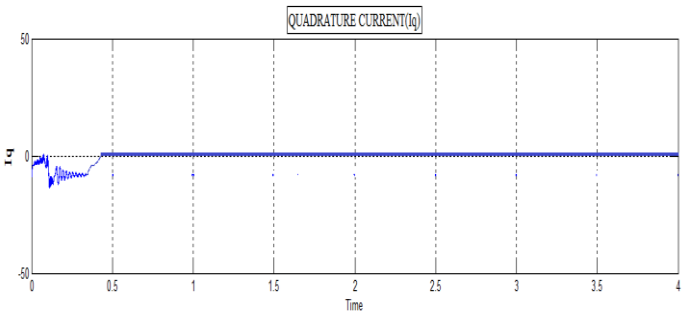
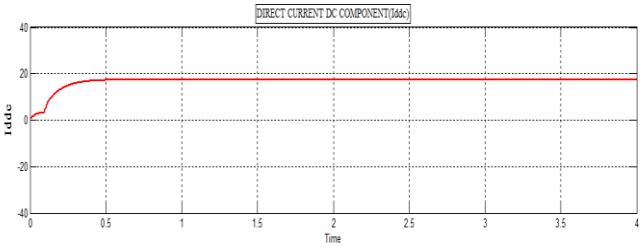


Fig.15 Transformed Currents of linear load.



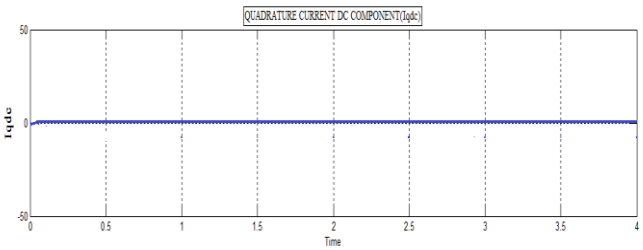


Fig.16 DC Component of the currents of linear load.

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Type of Load	Parameter	Without DSTATCOM	With DSTATCOM		
			Back Propagation Control Algorithm		*SRF theory*
			ZVR Mode	*PFC Mode*	
R load	Source Current(Amps) (Phase A)	13.87Amps	13.87Amps	13.87Amps	13.87Amps
	PCC Voltage(Volts) (Phase A)	238.9Volts	238.9Volts	238.9Volts	238.9Volts
	Load Current(Amps) (Phase A)	13.87Amps	13.87Amps	238.9Volts	238.9Volts
RL load	Source Current(Amps) (Phase A)	67.8 Amps	18 Amps	18.95Amps	21.93Amps
	PCC Voltage(Volts) (Phase A)	202Volts	237.8Volts	234.4Volts	230.3Volts
	Load Current(Amps) (Phase A)	67.8 Amps	18 Amps	18.95Amps	21.93Amps
RC load	Source Current(Amps) (Phase A)	87.6Amps	18.13Amps	19.65Amps	23,85Amps
	PCC Voltage(Volts) (Phase A)	291.9Volts	239.5Volts	243Volts	247.6Volts
	Load Current(Amps) (Phase A)	87.6Amps	18.13Amps	19.65Amps	23,85Amps

The generated reference source currents (isa*, isb*, and isc*) are compared to the sensed source currents (isa, isb, and isc), and current error signals are amplified through PI current regulators; their outputs are fed to a pulse width modulation (PWM) controller, which generates the gating signals for insulated-gate bipolar transistors (IGBTs) S1 to S6 of the VSC used as a DSTATCOM.

These generated pulses are given to their respective switches for the switching of DSTATCOM for the compensation. Compensating currents supplied by the DSTATCOM for reactive power compensation.

The outputs of the Simulink model are shown in Figures 17 and 18. Fig.17 shows the PCC voltage, load currents, and source currents. Fig.18 depicts DSTATCOM's DC link voltage. In this case, DC link voltage is retained at 700V.

As shown in Fig.17 from t=0.2sec to t=0.4sec i.e during RC load, source current, and PCC voltage, the load current is 23.85amps, 247.6volts, and 23.85amps respectively with Synchronous Reference frame theory when compared to 87.6amps, 291.9volts, and 87.6amps without DSTATCOM. And from t=0.5sec to t=0.7sec i.e during RL Load, Source current, and PCC voltage, the load current is 21.93amps, 230.3volts, and 21.93amps respectively when compared to 67.8amps,202volts, and 67.8amps without DSTATCOM. When loads are introduced at t=0.2sec and t=0.5sec, DSTATCOM either supplies or absorbs the reactive power and regulates the PCC voltage to a specific value.

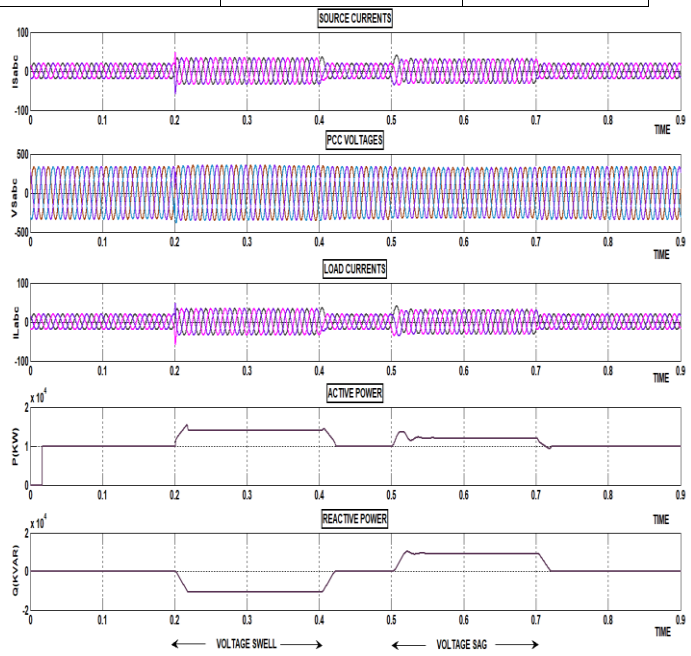

Fig.17 Output waveforms with DSTATCOM
(a)Source current, (b)PCC voltages, (c)Load currents(d)Active power(d)Reactive power

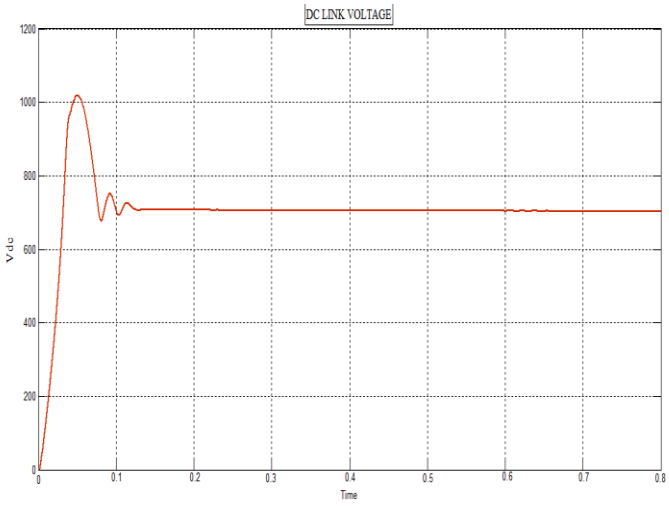

Fig.18 DC-Link voltage

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IV. CONCLUSION

In this paper performance of DSTATCOM is studied with the Back Propagation Control algorithm and SRF Theory for Voltage sag and Voltage swell compensation. Control algorithms based on DSATCOM are simulated with MATLAB using SIMULINK for different types of loads. The sinusoidal PWM technique is used for generating gating pulses. From Simulation Results, we concluded that DSTATCOM provides better performance with the Back Propagation control algorithm compared to SRF Theory. In the BP control technique Calculation of desired weights of the hidden layer is important.

The future work on this project can be carried out by using the space vector pulse width modulation technique and Hysteresis PWM technique for generating gating pulses for the switches and also by comparing this algorithm with other control algorithms like cross-correlation theory, sliding mode control, and symmetrical component theory, etc can be carried out and also by developing a hardware prototype model of DSTATCOM for Proposed Control algorithms, experimental analysis can also be done.

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