A Comparative Study of VLSI 3D Placement for Power Management and Wirelength Reduction

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***Abstract*— In recent days every application must need power management and area management such physical problems and aspects of VLSI design. Minimization of power and area are highly complex integrated systems in microelectronics have led to the 3 Dimension developments a technological approach. 3 Dimension offers numerous advantages: Size, power consumption, hybrid integration etc., various techniques to handle the power management in IC. Power dissipation in a IC is base on power used by the IC and also by heat dissipation. To reduce energy use or to minimize heat dissipation some of the techniques are available. Three-dimensional (3D) integration is a viable approach that allows designers to add functionality to the devices while maintaining the same die area without the need for new design process. Stack dies in 3D integrated circuits (ICs) also reduces the die area of designs. In addition, die area reduction helps decrease wire length, thus improving the performance of the designs.**

I. INTRODUCTION

The task of the very large scale integration (VLSI) placement is to assign exact location to various circuit components within the chip area. It involves number of objective such as wire length, area of the die, timing and power. Placement treats the shapes of all blocks as fixed; i.e., it only determines the location of each block on the chip. The variables are the xy locations of the blocks; most blocks are standard cells the y-locations of cells are restricted to standard-cell rows. Placement instance sizes range in to the tens of millions and will continue to increase. Placement is usually divided in to two steps: global placement and detailed placement .Global placement assigns blocks to certain sub regions of the chip without determining the exact location of each component within its sub region. As a result, the blocks may still overlap. Detailed placement starts from the result of global placement, removes all overlap between blocks, and further optimizes the design. Placement objectives include the estimated total wire length needed to connect blocks in nets, the maximum expected wiring congestion in subsequent routing, and the timing performances of the circuit. To solve such large scale mixed size VLSI placement problem. Many algorithms are used to solve the placement problem in VLSI among these algorithm

The placement algorithms are classified into constructive and iterative improvement methods. The constructive algorithm starts with the empty set and builds up the partition by adding one element at a time. These algorithms are faster but the quality of result is not good. An iterative algorithm starts with initial placements and repeatedly modifies it. These algorithms give good result but it takes long time.

The placement problems are, the wire length and area of the die , routability, power minimization and delay . Out of these mention problem the area minimization and the wire length minimization are the most critical part. For the area and wire length optimization a modern placer needs to handle the large-scale design with millions of object, heterogeneous object with different sizes and various constrained placement such as preplaced blocks and chip density. The traditional approach in placement is to construct an initial solution by using constructive heuristic algorithms. A final solution is then produced by using iterative improvement techniques where a modification is usually accepted if a reduction in cost occurs, otherwise it is rejected. The solution generated by constructive algorithms may be far from optimal. Thus an iterative improvement algorithm is performed next to improve the solution the computation time of such algorithm is also large.

This paper explains about the combination of techniques used for low power approach in integrated circuits (IC) or Chip and wire length minimization of a chip using 3D integrated circuits (ICs)

II. POWER MANAGEMENT

Power consumption is an important issue the semiconductor ecosystem is trying to address. It concerns electronic product providers across all segments. For example the power consumption in the CMOS device is major concern with Static power , Dynamic power and Short Circuit Power. Mainly two components determine the power consumption in a CMOS circuit Static power consumption and Dynamic power consumption, since Short Circuit Power Consumption is rarely occurred one. So the total power consumption for the a CMOS device is given by

$$P_{dissipation} = P_{static} + P_{dynamic} + P_{short\ circuit} \quad -2.1$$

The power Consumption for a single CMOS is approximately 5V. InVLSI fabrication billions of gate fabricated assume that how much power we needed to operate a single Chip.From this above analysis we know the awareness of power reeducation needed for the Integrated Circuits(IC).

Today, power and performance have become the predominant concerns for chip designers. Low power consumption is vital for handheld mobile and wireless devices as most of them are independent battery as the power source. Power management is becoming an increasingly urgent problem for almost every category of design, as power density (measured in watts per square millimeter) rises at an alarming rate.

The static power dissipation is due to reverse saturation, sub-threshold and leakage current and occurs especially when the device is in idle mode. The dynamic power dissipation occurs due to charging and discharging of load capacitance and short-circuit current when both the NMOS and PMOS devices remain ‘on’ for a short time duration

$$P_{switching} = afC_{eff}V_{dd} \quad -2.2$$

where ‘a’ is switching activity, ‘f’ is switching frequency, Ceff is effective capacitance and Vdd is supply voltage.

$$P_{short\text{-}circuit} = I_{sc} V_{dd} f \quad -- 2.3$$

where Isc is short-circuit current during switching, Vdd is supply voltage and ‘f’ is switching frequency. Dynamic power can be lowered by reducing the switching activity and clock frequency, which affects performance, and also by reducing the capacitance and supply voltage. Leakage power is a function of supply voltage Vdd, switching threshold voltage Vthand the transistor size

$$P_{Leakage} = f(V_{dd}, V_{th}, W/L) \quad -2.4$$

where Vddis supply voltage, V this threshold voltage, ‘W’ is transistor width and ‘L’ is transistor length

The performance of the IC is based on the circuit speed In general, "small area" and "high performance" are two conflicting constraints. The IC designers' activities have been involved in trading off these constrain. Power dissipation issue was not design criterion but an afterthought. In fact, power considerations have been the Ultimate design criteria in special portable applications such as wrist watches and pacemakers for a long time. The objective in these applications was minimum power for maximum battery life time.

There are so many numbers of ways to overcome this power consumption problem. In this further section of paper deals with the possible techniques available for the power management in an IC for long battery life .

III. METHODS OF POWER MANAGEMENT

Due to the increased circuit density and speed, the power dissipation has emerged as an important consideration in circuit design. A lot of efforts on power reduction have been made at various levels of design abstraction. Considering the fact that the charging/discharging of capacitance is the most significant source of power dissipation in well-designed CMOS circuits

Power consumption grows exponentially at 90nm and beyond technologies. At smaller geometries, aggressive management of leakage current can greatly impact design and implementation choices. Indeed, for some designs and libraries, leakage current exceeds switching currents, thus becoming the primary source of power dissipation in CMOS Depending upon the architecture of the design, the designers can choose from a wide range of options for reduction in power consumption of VLSI circuits. Some of the techniques to reduce the power consumption are briefed below.

There are several methodology are available for low power management for IC. Some of them are listed below and briefly discussed (1)Logic restructuring (2)Clock tree optimization and clock Gating (3)Logic resizing (transistor resizing).(4)Transition rate buffering.(5)Pin swapping (6)Using multi-threshold voltage (7)Multi-supply voltage (voltage islands)(8)Dynamic voltage scaling (9)Dynamic voltage and frequency scaling (DVFS)(10)Power shutoff or power gating (11)Memory splitting (12)Substrate biasing (body-biasing or back-biasing)(13)Operand isolation

From the above mention power management technique most of the popular used techniques are discussed and compare in this paper with respect to the power management issues in the 3D integration circuits

(i)Dynamic voltage scaling (ii)Dynamic voltage and frequency scaling (DVFS)(iii)Power shutoff or power gating

A. Dynamic Voltage Scaling

Dynamic voltage scaling (DVS) is a standard technique for managing the power consumption of a system. It is based on the fact that the dynamic (switching) power P of CMOS circuits is strongly dependent on the core voltage V and the clock frequency f according to

$$P \alpha f v^2 – 3.1$$

Under the assumption that the number of clock cycles required for a computation is independent of the core frequency, the execution time is inversely proportional to the frequency. The total energy E for the computation is then proportional to the square of the voltage:

$$E \alpha v\ 2 \text{ -- } 3.2$$

Note that the total energy for a computation is not depend on the frequency, but a reduced core voltage requires a reduction of the clock frequency and therefore implies a longer overall execution time. The assumptions behind Equation (2.8.2)are highly uncertain as they ignore other system components in particular the bus and memory. The other components impact the execution time of a program leading to a much more complex dependence on the processor frequency

B. Dynamic Voltage and Frequency Scaling

Dynamic Voltage and Frequency Scaling allows a host to dynamically switch its CPU frequency dependent on its load requirement. It do this by continuously monitoring the CPU utilization with the DVFS algorithm determining any necessary adjusts to the CPU’s frequency with the goal being to run the CPU at a lower frequency so that it consumes less power. It uses processor performance states (P-states) presented to the VM kernel through an ACPI interface to achieve this. For example: If your 2GHz CPU is sitting at 30% utilization then DVFS will reduce the frequency of the CPU so it will operate nearer to its 600MHz frequency requirement including enough headroom to accommodate a sudden increase in CPU requirement.

C. Power shutoff or power gating

Power Gating is effective for reducing leakage power. Power gating is the technique in circuit temporarily turned off the sub blocks to reduce the overall leakage power of the chip. This temporary shutdown time can also call as "low power mode" or "inactive mode". When circuit blocks are required for operation once again they are activated to "active mode". These two modes are switched at the appropriate time and in the suitable manner to maximize power performance while minimizing impact to performance. Thus goal of power gating is to minimize leakage power by temporarily cutting power off to selective blocks that are not required in that mode. Power gating affects design architecture more compared to the clock gating. It increases time delays as power gated modes have to be safely entered and exited. The possible amount of leakage power saving in such low power mode and the energy dissipation to enter and exit such mode introduces some architectural trade-offs. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is the other option.

An externally switched power supply is very basic form of power gating to achieve long term leakage power reduction. To shutoff the block for small interval of time internal power gating is suitable. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to

parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

The quality of this complex power network is critical to the success of a power-gating design. Two of the most critical parameters are the IR-drop and the penalties in silicon area and routing resources. Power gating can be implemented using cell- or cluster-based approaches or a distributed coarse-grained approach.

D. *Power-gating parameters*

Power gating implementation has additional considerations than the normal timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology .

- Power gate size
- Gate control slew rate:
- Simultaneous switching capacitance
- Power gate leakage

IV. PLACEMENT PROBLEM DESCRIPTION

A. *Area Estimation*

Given a set of module M_1, M_2,.....M_n and set of n interconnects N_1,N_2……N_n the objective of the placement is to obtain the non overlapping package of all the modules which achieves some optimization objective such as minimizing the area of package[3], the interconnection length as show in the below figure 1.

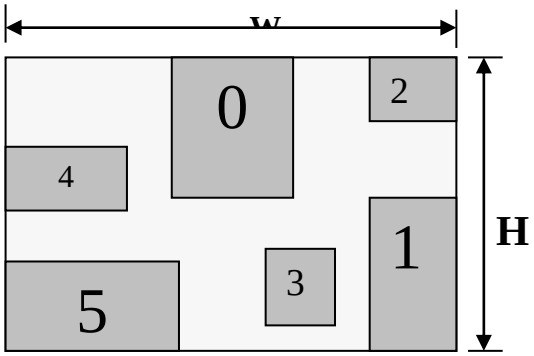


Figure 1. Placement Area Estimation

Horizontal constrain:

If (-X,Y) =(. . . a. . .b. . .,a. . . b. . .) Block b is is at right side of the block a

Vertical constrain:

If (X,Y) =(. . . a. . .b. . .,b .. . a. . .) Block b is at the below side of the block a

Based on "left of' constraint of (X, Y), a directed and vertex-weighted graph G_H (V, E) (V: vertex set, E: edge set), called the horizontal-constraint graph (HCG) is constructed as follows:

(1) V= {S_h} U {t_h} U|{b_i i = 1, . . . , M},

Where $\mathbf{b_i}$ correspond to the block

$\mathbf{S_h}$ is the source node representing the left boundary

$\mathbf{t_h}$ is the target node representing the right boundary

(2) E = {(S_h,b_i) i = 1,…,M} U {(b_i,t_h) i = 1,…,M} U {(b_i,b_j) ⊥.. b_i… b_j}

If existing, edge $\mathbf{(b_i,b_{i+1})}$ edge $\mathbf{(b_{i+1},b_{i+2})}$ and edge $\mathbf{(b_i,b_{i+2})}$ then $\mathbf{(b_i,b_{i+2})}$ omitted

3) Vertex Weight equals the width of the block b_i, but zero for $\mathbf{S_h}$ and $\mathbf{t_h}$ similarly the vertical constrain graph (VGH)

Vertical constrain graph G_v(V,E) is constructed using "above" constrain and the height of the each block. The corresponding constrain graph G_h(V,E) and G_v(V,E), Both G_h(V,E) and G_v(V,E) are vertex weighted acyclic graph so longest path algorithm can be applied to find the ***x*** and ***y*** coordinates of each block. The coordinates of the block coordinate of the lower left corner of the block.

B. *Wire length estimation*

We are addressing the problem of VLSI standardCell placement with the objectives of minimizing wire length , power consumption, and timing performance (delay), while considering the layout width as a constraint.

C. *Wire length measurement and Cost*

In VLSI placement the cells present in the module are connected by wire. The estimation of wire length [2] required for connection is calculated by the formula

$$\mathbf{Wire_{length}} = \sum_{I > j} \mathbf{w_{i,j}\,((x_i - x_j)^2 + (y_i - y_j)^2)}$$

Where

$\mathbf{w_{i,j}}$ weight of the connection between cell x and y

$\mathbf{(x_i - x_j)}$ distance in X direction

$\mathbf{(y_i - y_j)}$ distance in Y direction

Inter connect wire length of each net in the circuit is estimate during Steiner tree and then total wire length is computed by adding the individual estimates

$$\mathbf{Cost_{wire}} = \sum_{i \in M} \mathbf{l_i}$$

Where l is the wire length estimation for net i and M denotes total number of nets in circuit.

V. PLACEMENT ALGORITHMS

The philosophy of our tool follows that of its 2D counterpart, VPR .The flow of the TPR placement and routing CAD tool is shown in Figure 2. The placement algorithm first employs a partitioning step using the hMetis algorithm to divide the circuit into a number of balanced partitions, equal to the number of tiers for 3D integration. The goal of this first min-cut partitioning is to minimize the connections between tiers, which translates into reducing the number of vertical (i.e., inter-tier) wires and decreasing the area overhead associated with 3D switches as discussed in the previous section. After dividing the netlist into tiers, TPR continues with the placement of each tier using a hybrid approach that combines top-down partitioning and simulated annealing. The annealing step moves cells mostly within tiers. Finally, the cells are routed to obtain a placed and routed solution. The following sections describe these steps in more detail.

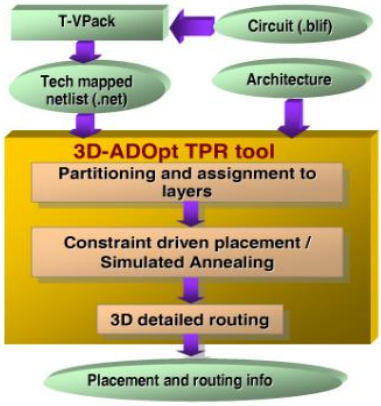


Figure 2. Flow of 3D TPR Tool

1) Partitioning the Circuit Between Tiers: The TPR step that performs partitioning and tier assignment of the circuit is shown conceptually in Figure 3. After the netlist is partitioned using hMetis, a novel linear placement approach is used to arrange the tiers such that wire length and the maximum cutsize between adjacent tiers is minimized. This is achieved by mapping this problem to that of minimizing the bandwidth of a matrix3 , using an efficient matrix bandwidth minimization heuristic.

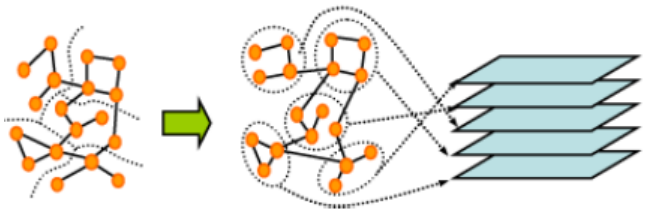


Figure 3. Partitioning of netlist in to Tires

2) Partitioning-based Placement Within Tiers: After the initial tier assignment, placement is performed on each tier starting with the top tier, proceeding tier after tier. The placement of every tier is based on edge-weighted quad-partitioning using the hMetis partitioning algorithm, and is similar to the approach in which has the same quality as VPR but at 34times shorter run times. Edge weights are usually computed inversely proportional to the timing slack of the corresponding nets. However, we also selectively bias weights of the most critical nets. The set of critical nets is comprised of edges on the current k-most critical paths. In order to improve timing, the bounding box of the terminals of a critical net placed on a tier is projected to the lower tiers and used as a placement constraint for other terminals. More details of the partitioning based placement phase can be found

A. *Transformations for 3D Placement*

The transformation schemes from a 2D placement to a 3D placement. Initial optimized 2D placement is done on a chip die of the 3D chip, where K is the number of dies, so that the total area of the 2D K times larger than a single placement is equal to that of the target 3D chip. Given this 2D placement with minimized wirelength, *local stacking transformation* can achieve even shorter wirelength for the same netlist with 3D integration. We also present two folding-based transformation schemes, *folding-2* and *folding-4*, which can generate 3D placement with a very low TSV number. Moreover, TSV number and wirelength tradeoffs can be achieved by the *window-based stacking/folding*. All these transformation methods can guarantee wirelength reduction over the initial 2D placement.

B. *Local Stacking Transformation*

Local stacking transformation (LST) consists of two steps, stacking and legalization, as shown in Figure 4. The stacking step shrinks the chip uniformly but does not shrink cell areas so that cells are stacked in a region K times smaller and remain as the original relative locations. The legalization step minimizes maximum on-chip temperature and TSV number through the position assignment of cells. The result of LST is a legalized 3D placement.

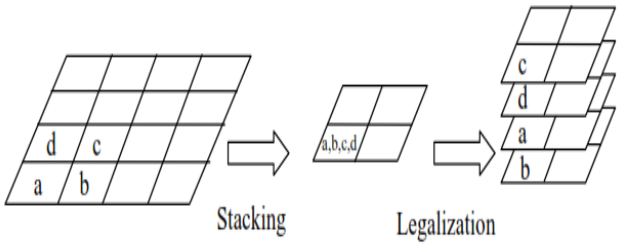


Figure 4. Local Staking Transformation

C. *Transformation through Folding*

LST achieves short wire length by stacking the neighboring nodes together. However, a great number of TSVs will be generated when the nodes of local nets are put on top of one another. If the target 3D integration technology only allows a limited TSV density, we need to use the transformations that generate fewer TSVs. Folding-based transformation is to fold the original 2D placement like a piece of paper without cutting off any parts of the placement. The distance between any two nodes will not increase and the total wire length is ***guaranteed*** to decrease. TSVs are only introduced to the nets crossing the folding lines With an initial 2D placement of minimized wire length, the number of such long nets should be fairly small, which implies that the connections between the folded regions should be limited, resulting in much fewer TSVs (compared to that of the LST transformation, where many dense local connections cross different dies). shows one way of folding, named folding-2, by folding twice at both x and yanother way of folding, named folding-4, by folding twice at both x and y directions. The folding results are legalized 3D placements, so no legalization step is necessary. After folding-based transformations, only the lengths of the global nets that go across the folding lines (dotted lines in Figure 5) get reduced. Therefore, folding-based transformations cannot achieve as much wire length reduction as LST. Furthermore, if we want to maintain the original aspect ratio, folding-based transformations are only applicable to the 3D design with an even number of dies.

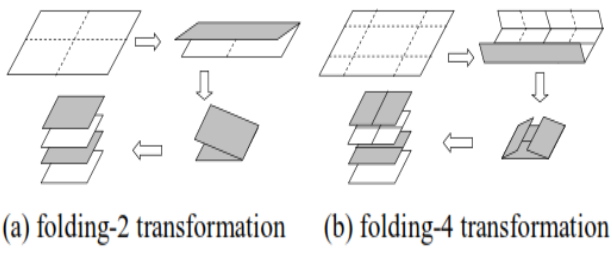
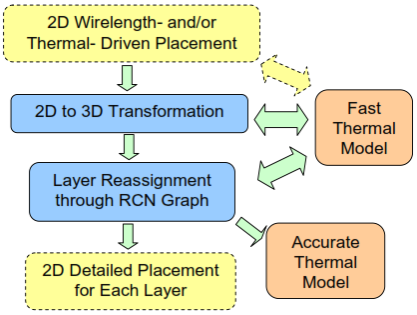


Figure 5. Folding Based Transformation schemes

VI. CONCLUSION



By using the transformation based 3D placement algorithm. The components with a dashed boundary are the exiting tools that we use. A 2D wire length thermal driven placer, force driven placement or memetic algorithm based placer is first used to generate a 2D placement for the target design. the quality of the final 3D placement highly depends on the initial placement . the 2D placement is then transform in to legalized 3D placement according to the already discussed 3D technology in the above paper during the transformation wire length , TSV number must be consider. A refinement process through die reassignment will be carried out after 3D transformation to further reduce the TSV number and bring down the maximum on chip temperature. Finally a 2D detailed placer will further refine the placement result for each die

As technology shrinks feature sizes, reliability will dominate as a design consideration .Die area (manufacturing cost) and performance (heavily influenced by cycle time) are important basic design considerations. Power consumption has also come to the fore as a design limitation. As technology shrinks feature sizes, reliability will dominate as a design consideration. the sizes of die decrease in future , so do device sizes. Smaller device sizes result in reduced capacitance. Decreasing the capacitance decreases both the dynamic power consumption and the gate delays. As device sizes decrease, the electric field applied to them becomes destructively large. To increase the device reliability, we need to reduce the supply voltage V. Reducing V effectively reduces the dynamic power consumption, but results in an increase in the gate delays. We can avoid this loss by reducing Vth. On the other hand, reducing Vth increases the leakage current, and therefore, the static power consumption. Determining performance is relatively straightforward when compared with the determination of overall cost. A good design achieves an optimum cost–performance tradeoff between the power and area . This determines the quality of a processor design

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