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A Comparative Study Of SOI-MOSFET Modelling Structure And Their Characterisation Through Simulation TCAD Tool

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***Abstract*— In this project we present the modelling of SOI-MOSFET through simulation TCAD tool in micrometer dimensions called SILVACO-ATLAS. This simulation tool is used for modelling of different types of semiconductor devices. SILVACO is a 2D virtual wafer fabrication tool where many simulators are present within it. The main simulators are Atlas and Athena etc. SOI Technology follows after CMOS devices. The major problems associated with CMOS devices are Degraded subthreshold slope, Parasitic capacitance and Latch up effect .SOI-MOSFET is a Silicon on Insulator (SOI) metal oxide semiconductor FET structure where a semiconductor layer e.g. silicon, germanium or the like is formed above an insulator layer which may be a buried oxide (BOX) layer formed in a semiconductor substrate. The characteristics of SOI-MOSFET can be studied by varying thickness of either silicon layer or oxide layer and the effect of change in threshold voltage values. Different characteristics curves between voltage and current, capacitance and voltage and thickness in silicon layer and threshold voltage etc. Different structures were modelled in SILVACO-Atlas. All these curves are obtained from these different structures of SOI-MOSFET devices. The advantages of using SOI-MOSFET device to remove high parasitic capacitance values and latch effect thereby improving performance. This SILVACO software will provide all types of device modelling with low-cost and easily available simulators successfully.**

***Keywords*—SOI-MOSFET, Latch effect, CMOS, Parasitic capacitance.**

I.INTRODUCTION

The market has been growing and making tough demands for semiconductor integrated circuits, which are mounted components, to consume less power, have higher integration, have multi-function capability, and be faster. We in this paper are presenting complete depletion type SOI devices in order to meet these needs. This article explains SOI-CMOS device technology and discusses current developments. In electronics , an SOI MOSFET semiconductor device is a Silicon on Insulator (SOI) MOSFET structure in which a semiconductor layer e.g.,silicon , germanium or the like , is formed above an Insulator layer which may be a buried oxide (BOX) layer formed in a semiconductor substrate. The use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing. It differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or sapphire . In SOI technology small islands of silicon are formed on an insulator film. Using SOI fabrication process coupled with lateral isolation techniques we can get circuits with very small parasitic capacitances and latchup free circuits. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects. One of these parasitic is the capacitance between diffused source and drain and substrate. This capacitance increases with substrate doping and becomes larger in modern submicron devices where doping concentration in the substrate is higher than in previous MOS technologies .In addition latchup effect can be reduced by using SOI-MOSFET .The SOI-MOSFET device contains the traditional three terminals (source ,drain and gate which controls a channel in which current flows from source to drain). So the figure shows the basic structure of a SOI-MOSFET with grain ,source and drain terminals .The dimensions of this structure are followed for proper modelling of the structure.

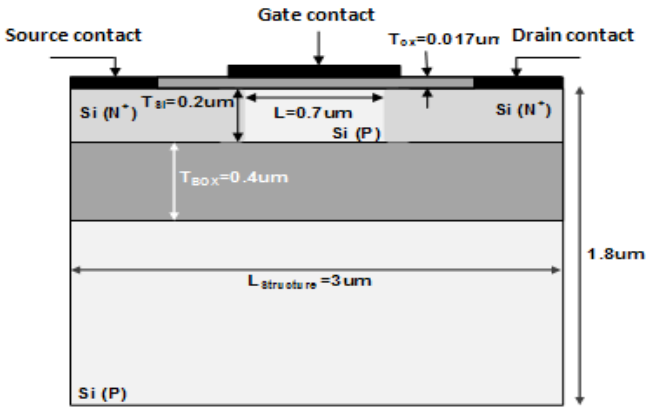

Fig. 1 Cross-sectional figure of SOI-MOSFET

The above fig1 shows the cross sectional figure of SOI-MOSFET structure with different layers thereby following dimensions in micrometer .These dimensions play an important in further study of device characteristics of these structures. The specifications of the above SOI-MOSFET are:

Drain and Source length=1um
Gate length= 1um
Channel length=1um

Gate oxide thickness TOX=0.017um
Silicon film thickness tsi=0.2um
Buried oxide thickness TBOX= 0.4um
Substrate thickness=1.2um
Depth junction=0.52um
Substrate doping=1x10^17cm-³
Drain and Source doping=1x10^20cm-³

II.EXPERIMENTAL MATERIALS AND METHODS

We know the real-time fabrication methods for SOI-MOSFET device .First of all the silicon substrate of SOI-MOSFET device was modelled by followed by thick oxide layer which is an insulator with again with another silicon layer are made using Atlas-simulator (SILVACO). The thick silicon dioxide layer is also known as the Buried Oxide layer (BOX) .The silicon layer above the BOX is where the device is fabricated , and the silicon underneath the BOX, can handle the wafer during fabrication process, and does not affect device performance to any great degree. All the three terminals i.e gate, drain and source are shown .This structure will help to find out simulated outputs.

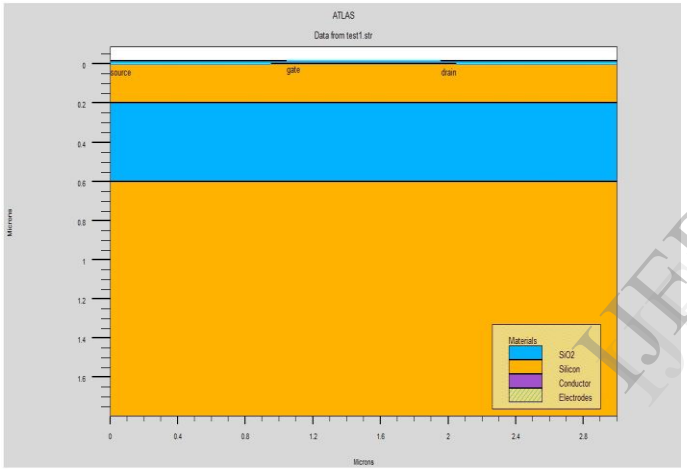

Fig2: SOI-MOSFET structure in Atlas simulator

Apart from the designing concept ,the SOI-MOSFETs comes with many device related fabrication problems .Those are-Kink effect ,Lattice heating and Subthreshold slope etc .The kink effect is characterized by the appearance kink in the output characteristics of an SOI-MOSFET. The kink appears above a certain drain voltage. SOI-MOSFETs are thermally insulated from the substrate by the buried insulator.SOI MOSFET's are thermally insulated from the substrate by the buried insulator.This arises because device is thermally insulated from the substrate by a burried oxide layer. Leads to substantial elevation in temperature which affects the output. This effect is called as Lattice heating. These problems can be reduced by varying the thickness tsi of silicon layer of SOI-MOSFET.

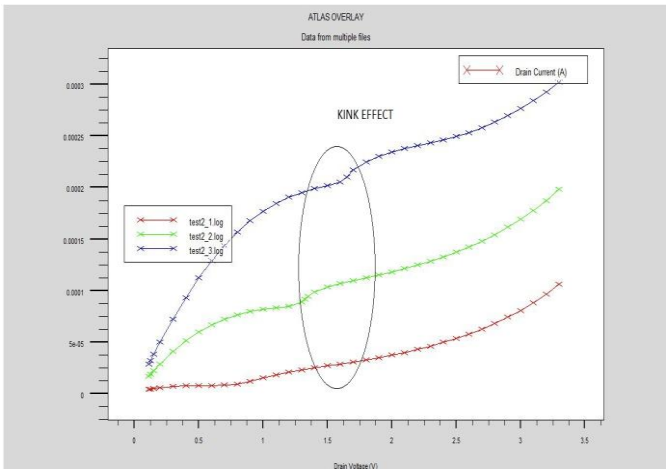

Fig3: Kink effect in SOI-MOSFET device

II.SIMULATED RESULTS

For computer simulations of the Silicon-on-Insulator device , where first was the Deckbuild software that ran the code, and provides the interface for changing and altering the code. Atlas allowed us to create a simplified version of the SOI device in which it was easy to vary parameters such as gate length and doping.etc .The first step is to model the structure with proper dimensions then voltage will be applied to the gate for determination of I-V curves.

For this we need to write the code for obtaining I-V curves that is Id-Vds (Fig 3) and Id-Vgs (Fig 4) as shown below:

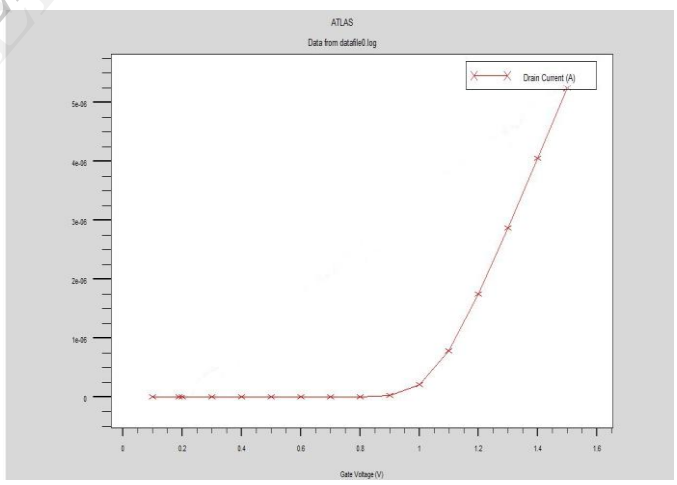

Fig.4 (Id-Vgs) Current-voltage characteristics of SOI-MOSFET

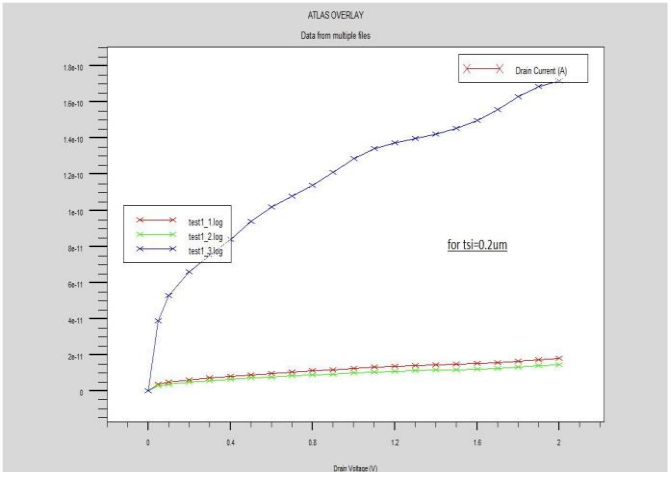

Fig.5 (Id-Vds) Current-voltage characteristics of SOI-MOSFET

IV. Simulated Results with Discussions

Here after simulation we can see the further change in the I-V characteristics by varying the change in silicon layer thickness tsi. This change will show the effects further in threshold voltages. By reducing the tsi thickness threshold voltage Vth also gets reduced. We can see the different change in current and voltage characteristics by varying the silicon layer thickness with tsi=0.2um, 0.1um and 0.05um.This shows that the more threshold voltage values are reduced we find further reduction in the threshold voltage values from the figures below.

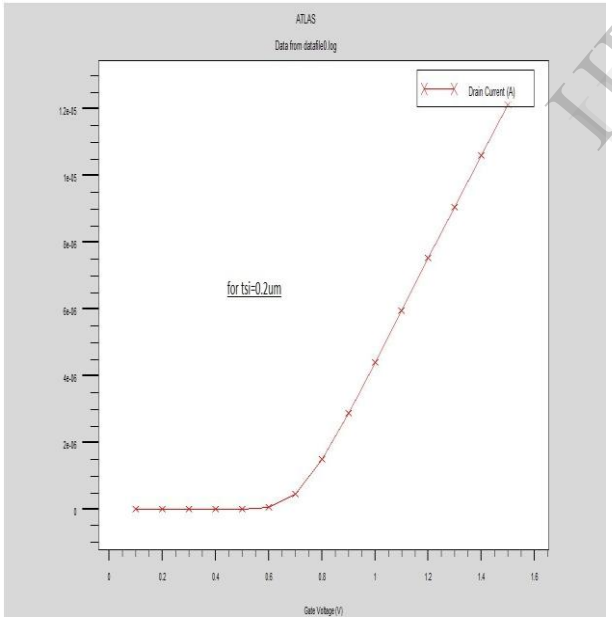

Fig. 6: Current-Voltage characteristics of SOI (Id-Vgs)(with tsi=0.2um)

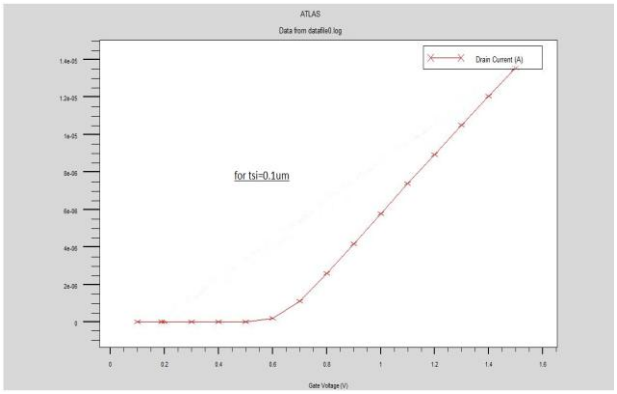

Fig. 7: Current-Voltage characteristics of SOI (Id-Vgs) (with tsi=0.1um)

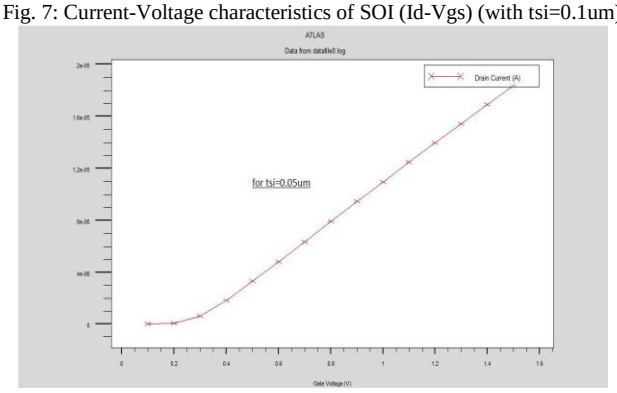

Fig. 8: Current-Voltage characteristics of SOI (Id-Vgs) (with tsi=0.05um)

Similarly the change in Id-Vds graph we can able to see the change in silicon layer thickness (Tsi) with those above mentioned values.

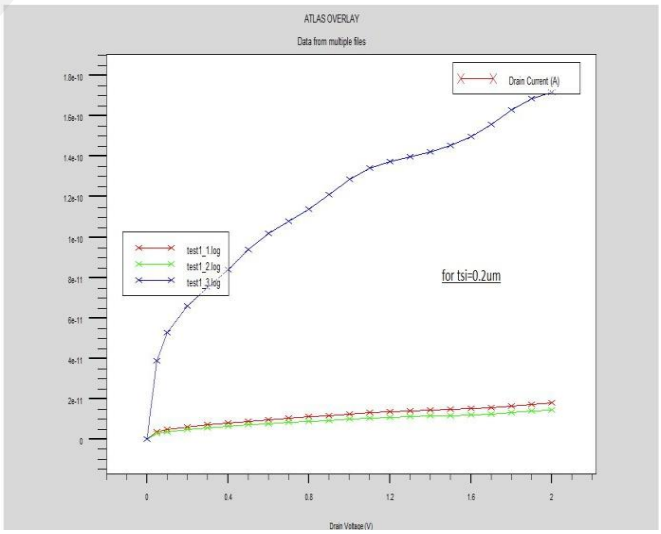

Fig. 9: Current-Voltage characteristics of SOI (Id-Vds) (with tsi=0.2um)

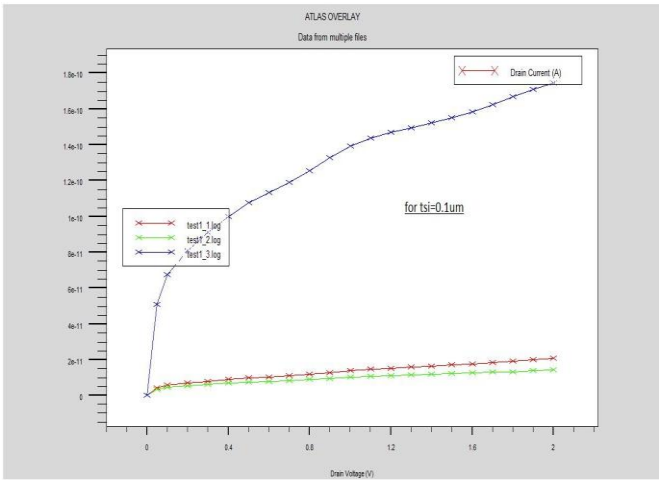

Fig. 10: Current-Voltage characteristics of SOI (Id-Vds) (with tsi=0.1um)

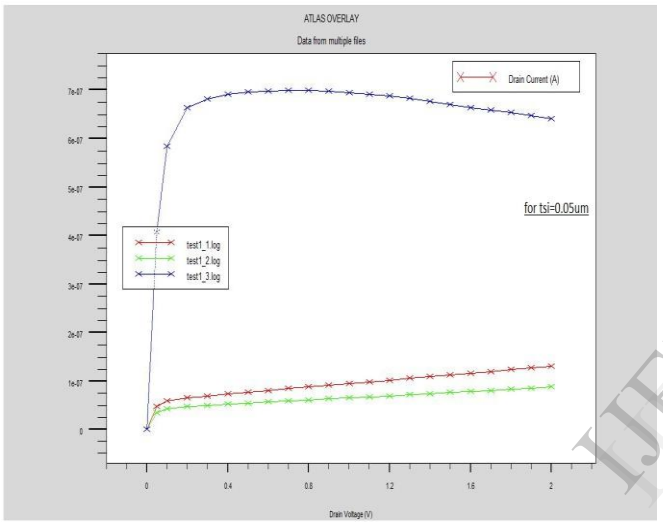

Fig.11: Current-Voltage characteristics of SOI (Id-Vds) (with tsi=0.05um)

We can see the same change in the Id-Vds graph where the change in saturation point occurs. The more decrease in silicon layer thickness the saturation point reaches faster and a much reduction in threshold voltage was found to be seen. This decrease in threshold voltage is advantageous in case of SOI-MOSFET so that kink effect problem can be reduced to some extent. This simulated graphs gives a solution for removing Kink effect. From these graphs it is concluded that it is better to keep lower tsi to reduce the kink effect and threshold voltage.

Similarly if we vary the gate oxide thickness (Tox) the effective change in threshold voltage was found to be seen with different varying thickness values i.e 0.01um,0.001um and 0.005um respectively. The figures below shows the change in Id-Vgs and Id-Vds with change in oxide thickness

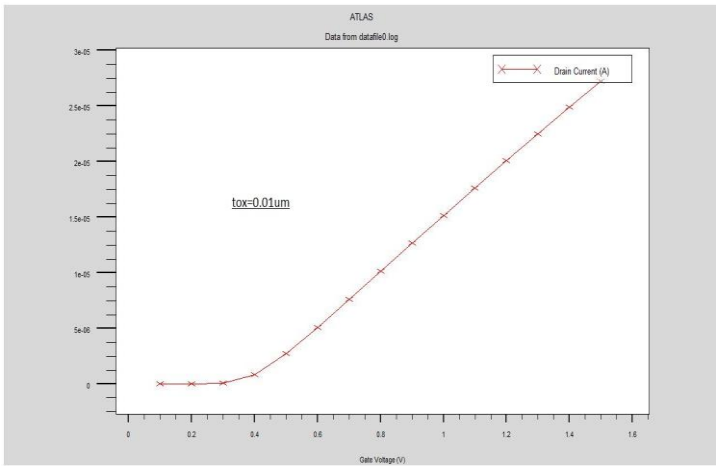

Fig.12: Current-Voltage characteristics of SOI (Id-Vgs) (with tsi=0.01um)

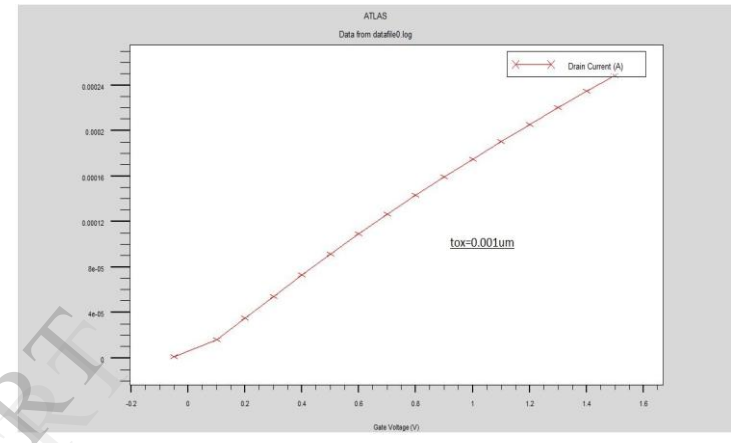

Fig.13: Current-Voltage characteristics of SOI (Id-Vgs) (with tsi=0.001um)

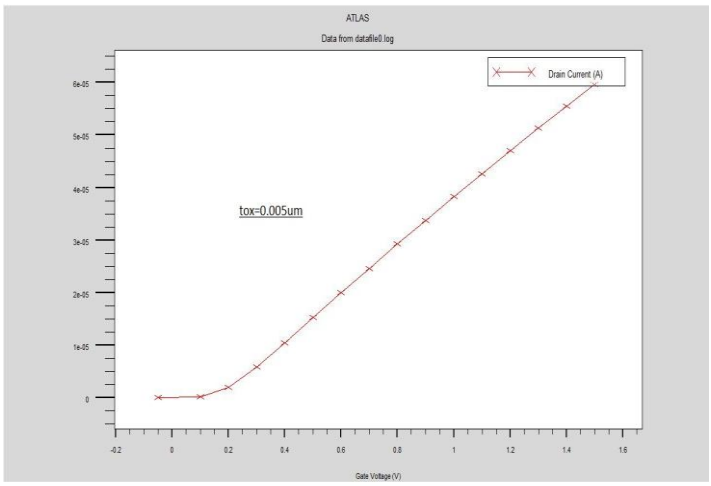

Fig.14: Current-Voltage characteristics of SOI (Id-Vgs) (with tsi=0.05um)

We can see the same change in the Id-Vds graph where the change in saturation point occurs. The more decrease in oxide layer thickness the saturation point reaches faster and a much reduction in threshold voltage was found to be seen. This

decrease in threshold voltage is advantageous in case of SOI-MOSFET so that kink effect problem can be reduced to some extent. This simulated graph gives a solution for removing Kink effect. From these graphs it is concluded that it is better to keep lower tsi to reduce the kink effect and threshold voltage.

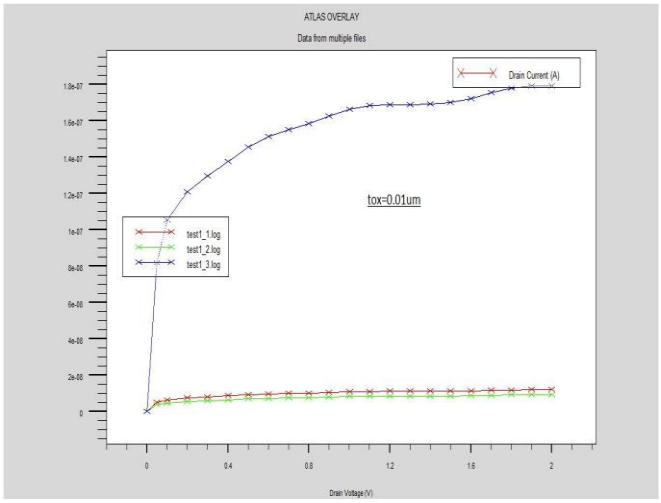

Fig.15: Current-Voltage characteristics of SOI (Id-Vds) (with tsi=0.01um)

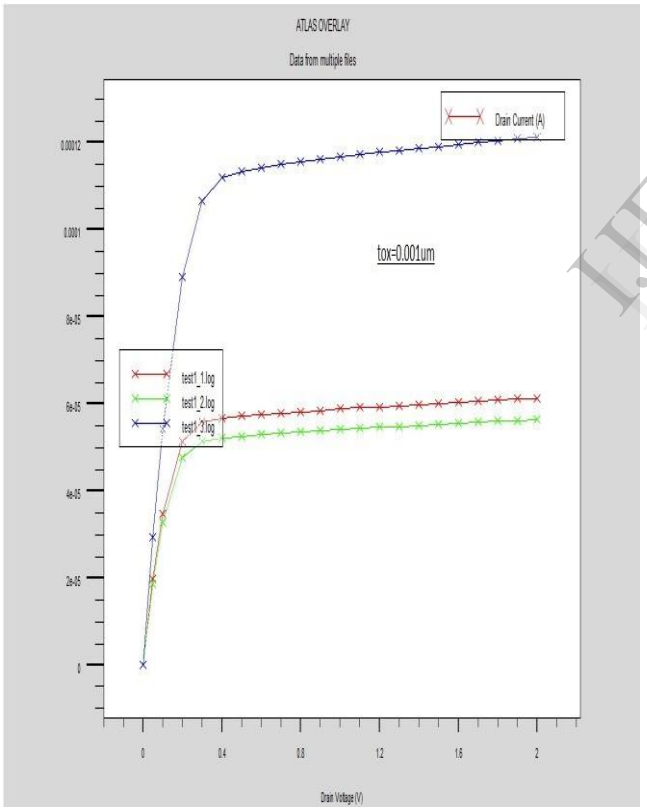

Fig.16: Current-Voltage characteristics of SOI (Id-Vds) (with tsi=0.001um)

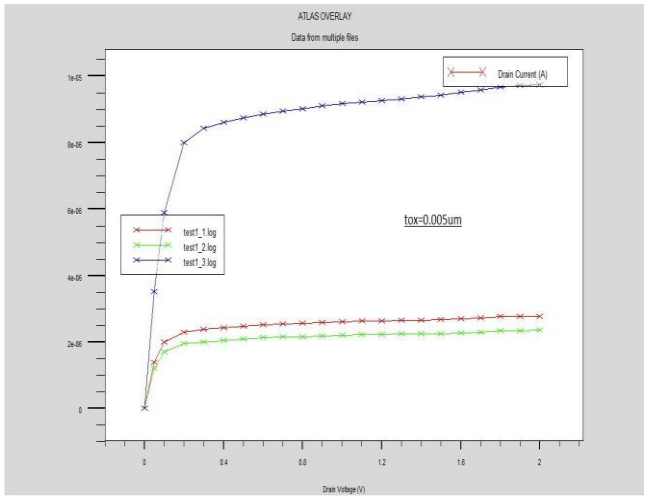

Fig.17: Current-Voltage characteristics of SOI (Id-Vds) (with tsi=0.005um)

Sillicon layer thickness (tsi)	Threshold Voltage (Vth)	RESULT	PARAMETERS
0.2um	0.64V	Tsi decreases Vth decreases	Gate Length=1um Source length=1um Drain Length=1um Buried Oxide thickness-0.4um Substrate Thickness=1.2um Doping=1.2*10^20
0.1um	0.6V		
0.05um (fully depleted)	0.05V		

Fig 18: Table showing the change in oxide layer thickness along with changed Vth changes

oxide layer thickness	Threshold voltage	Result
0.01um	0.4v	Tox decreases , Vth decreases
0.001um	0.1v	Tox decreases , Vth decreases
0.005um	0.2v	Tox decreases , Vth decreases

Fig 19: Table showing the change in silicon layer thickness along with changed Vth changes

V. CONCLUSIONS

The above project is initiated to make use of these TCAD tools for designing and modelling SOI devices using fabrication methods and proper characterisation of SOI devices by usage of Simulation tools. It fulfils the objective to those that are followed by using real time fabrication methods which of high cost and complex in carrying –out the processes. The study and learning of tools successfully makes the system easy in determining and visualising the results. The knowledge of different materials plays a key role in the fabrication of these devices. The science dealing with the study of properties of materials is Material Science. This itself has made it possible the fabrication, modeling and simulation of these semiconductor devices. The availability of low-cost simulation tcad tools helps us in determining design specific parameters and makes them possible for fabrication in future out the structures and model in technological oriented simulation tools like SILVACO .The low-cost technological processes has motivated the researchers to go for implementation of semiconductor devices using such design tools. These methods can fulfill the objective of carrying –out the processes with new and advanced semiconductor devices. The dip-coating method helps out in development and running of devices in simulated form. As the mechanism are cost-effective and easily available.

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