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A Comparative Study of Costas Loop and DPLL for Carrier Synchronization

Chinchu V
Dept. of Electronics and Communication Engineering
Manipal University Jaipur,
Jaipur, India.

Mrs. Madhuri Sahal
Assistant Proffesor,
Dept. of Electronics and Communication Engineering
Manipal University Jaipur,
Jaipur, India

***Abstract*—This paper presents comparison of a simple costas loop and DPLL for carrier recovery. Synchronization is basically the process of frequency and phase aligning of remote oscillators. The first task is carrier acquisition which includes forming a frequency and phase-matched replica of the local oscillator for the process of down conversion. A local oscillator in detector is forced to oscillate in both phase and frequency with respect to the carrier oscillator at the transmitter. Timing recovery is the second task focused on collecting a set of aligned input samples time and the replica template.**

The presence of carrier phase error causes signal to rotate. For larger rotation, the symbol signal space projections lie in a wrong decision region. Hence there occurs a decision error even if a perfect timing recovery scheme is applied for zero additive noise. Carrier synchronization aims to detect the phase of carrier. Simulation results are presented for evaluating the behavior of costas loop and DPLL.

***Keyword*—Synchronization, Carrier recovery, Costas loop, DPLL, Frequency estimator, Phase Estimator**

I.INTRODUCTION

Generally transmitted signal is modified by the channel. Here the channel is assumed to be an additive white Gaussian noise (AWGN) channel. A delay also occurs at the receiver due to the time required for propagation of signal. It leads to sampling at instances in suboptimal time. Along with the relative movement between the transmitter and receiver causes a Doppler shift, imperfections in their local oscillators also tend signal to rotate in the signal space by a constant frequency offset [5].

The received signal is hence a modified version of transmitted signal due to these effects. The role of synchronizer is to estimate the fequency offset and delay occurred at channel, along with the phase offset and then to remove or reduce these modifications. Sent data symbols are then detection by the synchronizer [7].

II. THE COSTAS LOOP

In today's fast paced world, increase in the communication systems demand for high data rate tends operating frequency to millimeter wave region. Hence with modulation schemes like ASK and PSK, high data rate at larger bandwidth is applicable.

Communication system has a hierarchy of synchronization problem when dealing with these high data rates and high frequencies is the problem of carrier recovery. Synchronizer detection includes recovery of carrier offset present in RF signal with respect to a reference phase and frequency.

Baseband signal requires high speed A/D-converters which in turn increases power consumption as well as design complexity [7]. For frequency exceeding several GHz, delay line will be in tens of millimeters. The length of delay elements determines the data rate [8]. For BPSK signal circuit is required which works with twice the carrier frequency since a frequency multipler is used. Hence for millimeter range of frequency costas loop is used [6].

A. Operation

J. Costas proposed the Costas loop as a phase tracker for AM signals [9, 5] which was later modified to demodulate PSK signals [2], [6].The operation of the Costas loop is shown in Fig. 3.

BPSK modulated RF signal X is given by:

$$X = I(t)\sin(\omega t + \theta) + Q(t)\cos(\omega t + \theta) \quad (1)$$

Where I(t) and Q(t) are symols having value of ±1, which varies at symbol rate. This signal is then passed through a multiplier which multiplies signal with LO of same frequency and an instantaneous phase of θ′ and a LO with 90◦ phase shift. After passing through loop filter the signals are:

$$Z_I(t) = I(t)\cos\varphi - Q(t)\sin\varphi \quad (2)$$

$$Z_Q(t) = I(t)\sin\varphi + Q(t)\cos\varphi \quad (3)$$

With $\varphi = \theta - \theta'$. The Output of the limiters for phase error of $|\varphi| < 45^{\circ}$ is:

$$L_I(t) = I(t) \quad (4)$$

$$L_Q(t) = Q(t) \quad (5)$$

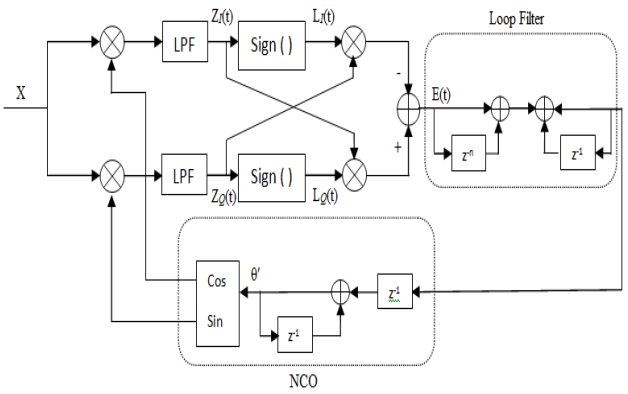

Fig .3. Schematic of discrete time equivalent of costas loop

The error signal is given by:

$$E(t) = Z_Q L_I - Z_I L_Q$$

$$= I^2(t)\sin\varphi + Q(t)I(t)\cos\varphi - I(t)Q(t)\cos\varphi + Q^2(t)\sin\varphi$$

$$= 2\sin\varphi$$

$$\approx 2\varphi \text{ (for very small } \varphi) \quad (6)$$

Hence, a phase error signal is obtained, along with VCO adjustment for maintaining the phase and frequency lock.

III. DPLL

The role of PLL is to synchronize the received signal frequency and phase using a feedback control circuit. Using negative feedback it locks the frequency and phase of the signal. DPLL is a modified PLL which contains a frequency estimator for estimation of large frequency offset followed by a phase estimator for phase estimation. This scheme overcomes the drawbacks of costas loop and PLL such as narrow frequency tracking, high frequency ripple and overshoot. The DPLL frequency estimator has the ability for high accuracy estimation of frequencies with large range that is from zero to half the sampling frequency. The output of frequency estimator is then used to control a phase estimator, a low noise PLL. Fig. 4 shows the complete structure of this mechanism. The output of this structure is the estimated phase and the estimated frequency.

A. *Frequency Estimator*

Fig. 5 shows the block diagram of the DPLL frequency estimator. It resembles a PLL structure except that the phase detector in PLL is changed to frequency detector, LPF to an accumulator and VCO to a quadrature numerically controlled oscillator (NCO) [1]. The frequency detector component consists of multipliers, adders, subtractors, differentiator and squaring circuit. Discrete time implementation of frequency estimator is explained in Fig. 5. Mathematical expressions for frequency estimator, stability and power estimator is provided here [4].

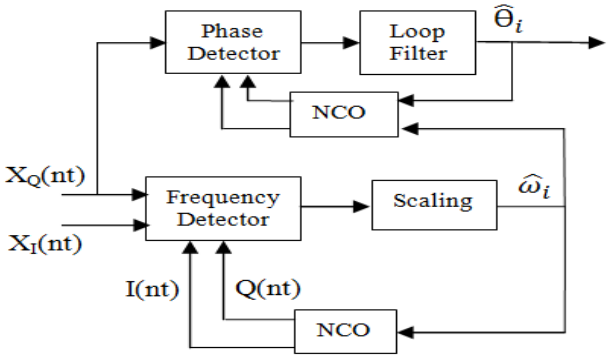

Fig 4. Operation of DPLL architecture.

B. *Frequency estimation*

The input signal and the signal generated by the oscillator are:

$$X_I(t) = \cos(2\pi fct + \theta_i) \quad (7)$$

$$X_Q(t) = \sin(2\pi fct + \theta_i) \quad (8)$$

$$I(t) = \cos(2\pi fot + \theta_o) \quad (9)$$

$$Q(t) = \sin(2\pi fot + \theta_o) \quad (10)$$

Where fc, f_o, θ_i and θ_o are input and output frequencies and phases respectively, t is the sampling time.

Multiplication of both the input signal with both the signals generated by oscillator result in two quadrature signals ($Rx_I(t)$, $Rx_Q(t)$) given as:

$$R_{X_I}(t) = X_I(t)I(t) + X_Q(t)Q(t)$$

$$= \cos(2\pi\Delta ft + \Delta\theta), \quad (11)$$

$$Rx_Q(t) = X_I(t)Q(t) - X_Q(t)I(t)$$

$$= -\sin(2\pi\Delta ft + \Delta\theta) \quad (12)$$

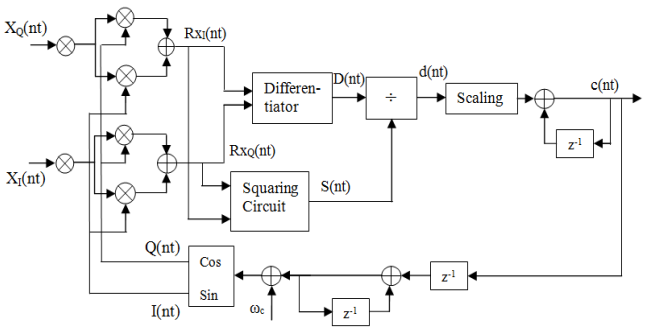

Fig. 5. Discrete time model of Frequency estimator.

Where $\Delta f = f_c - f_o$, $\Delta\theta = \theta_i - \theta_o$. The quadrature signals (Rx_I (n), Rx_Q (n)) is then passed through differentiator circuit.

$$\frac{d}{dt}Rx_I(T)|_{T=nt} \approx \{Rx_I(nt) - Rx_I((n-1)t\} \times \frac{1}{t}$$

$$= -2\pi\Delta f \sin(2\pi\Delta fnt + \Delta\theta) + \cos(2\pi\Delta fnt + \Delta\theta) \quad (13)$$

$$\frac{d}{dt}Rx(T)|_{T=nt} \approx \{Rx_Q(nt) - Rx_Q((n-1)t\} \times \frac{1}{t}$$

$$= -2\pi\Delta f \cos(2\pi\Delta fnt + \Delta\theta) - \sin(2\pi\Delta fnt\Delta\theta) \quad (14)$$

The differentiator output is

$$D(nt) = Rx_Q(nt) \times \frac{d}{dt} Rx_I(T)|_{T=nt}$$

$$= 2\pi\Delta f[sin^2(2\pi\Delta fnt + \Delta\theta) + cos^2(2\pi\Delta fnt + \Delta\theta)]$$

$$= 2\pi\Delta f = \Delta\omega \quad (15)$$

The signals (r_I (n), r_Q (n)) also at the same time passes through squaring circuit. The output of squaring circuit can be considered as power of input signal.

$$S(nt) = Rx_I{}^2(nt) + Rx_Q{}^2(nt)$$

$$= [sin^2(2\pi\Delta fnt + \Delta\theta) + cos^2(2\pi\Delta fnt + \Delta\theta)]$$

$$= 1 \quad (16)$$

The output of divider is

$$d(nT_s) = \frac{D(nT_s)}{S(nT_s)} = \Delta\omega \quad (17)$$

The scaling of frequency difference is done until the frequency generated by oscillator and input frequency becomes same.

The scaled output is

$$\mu d(nt) = c(nt) - c((n-1)t). \quad (18)$$

Where, μ is a variable which controls stability of the system. Its range is $0 \leq \mu < 1$. For small values of μ, the system is more stable but takes long settle time, for greater values of μ settling time decreases.

Output of accumulator controls NCO output. Feedback loop in estimator continues until input frequency and frequency generated by NCO becomes equal.

The NCO equation is

$$f_o(nt) = f_c + \sum_{k=0}^{n-1} c(kt) \quad (19)$$

Where, f_c is the center frequency. Accumulator saturates as soon as the NCO generated frequency and input frequency becomes equal.

Hence at ω_i (nt) = ω_0 (nt);

$$c(nt) = \omega_i t = 2\pi f_c t = \omega_c t \quad (20)$$

C. Phase Estimator

A low noise DPLL phase detector is used here [3]. A simple PLL cannot remove completely high frequency ripples that are present in signal.

The aim of DPLL structure is to use a first order LPF which provides system stability along with the ability to remove the ripples.

$$s_d(nt) = k_d\{sin(\omega_i nt + \theta_i) - sin(\hat{\omega}_i nt + \hat{\theta})\} \times cos(\hat{\omega}_i nt + \hat{\theta}) \quad (21)$$

Where $\hat{\omega}_i$ and $\hat{\theta}$ are radian frequency and phase of signal generated from NCO respectively, k_d is the multiplier gain. First stage estimates the frequency. So at $\omega_i = \hat{\omega}_i$,

$$s_d = \frac{k_d}{2}\{\sin(2\omega_i nt + \theta_i + \hat{\theta}) + sin(\theta_i - \hat{\theta}) - n(2\omega_i nt + 2\hat{\theta})\} \quad (22)$$

From (22) from the high frequency is subtracted by a new term before passing to LPF. Hence, the LPF in this mechanism have to remove only the residual of subtraction in turn of removing entire high frequency term as in a simple PLL. Hence, the first order LPF removes the residual and enhances the stability of DPLL. The resulting signal from LPF is:

$$s_i(nt) = \frac{k_d}{2} sin(\theta_i - \hat{\theta}) \quad (23)$$

At $(\theta_i - \hat{\theta}) << 1$, then

$$s_i(nT_s) = \frac{A_i A_o k_d}{2}(\theta_i - \hat{\theta}) \quad (24)$$

This signal controls the phase of NCO generated signal, and the DPLL continues the variation of the phase until locking occurs and $\theta_i = \hat{\theta}$.

IV. RESULT ANALYSIS

Simulations are carried out for comparing the working of costas loop and DPLL for receiver synchronization.

The performance of costas loop carrier synchronization mechanism for a simple BPSK signal is illustrated. The input signal is set at a carrier frequency f_c of 500 KHz and sampling frequency fs = 1/t as 20MHz. BPSK signal with 100 samples are generated.

Close view of the synchronized received signal is shown in fig. 6. The constellation diagram of received signal is shown in fig. 7.

The comparison of receiver synchronized signal with a generated signal along with some offset is given in Fig. 8. In Fig. 8, signal plotted in blue is input signal and the signal plotted in red shows the synchronized received signal

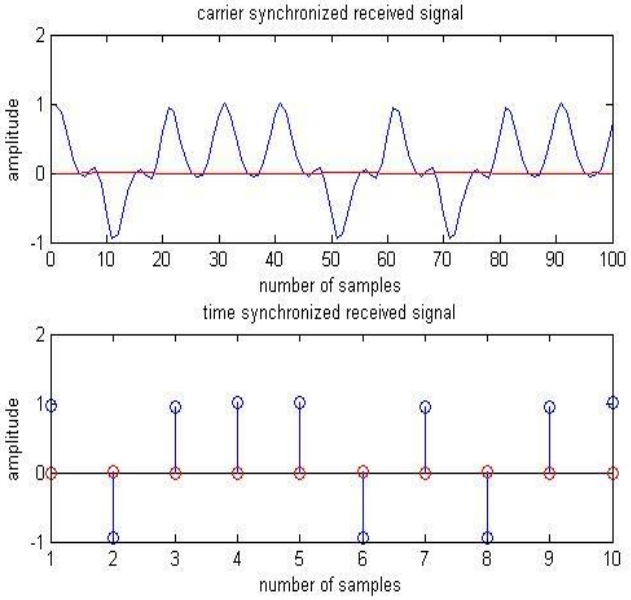

Fig. 6. Carrier synchronised received signal, blue shows reiceved signal and red shows error signal

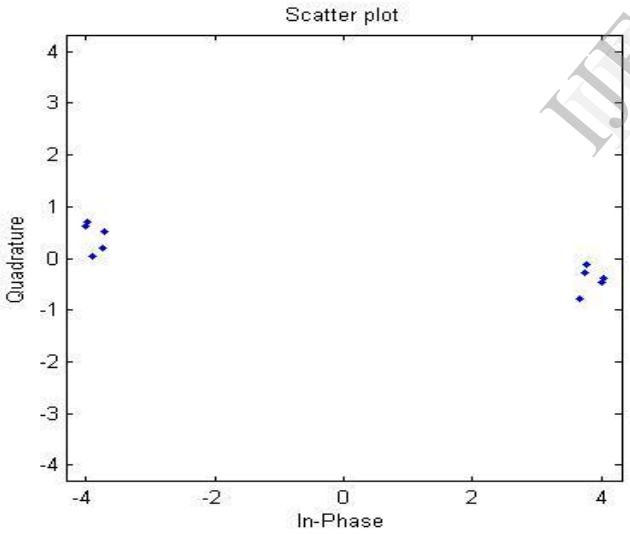

Fig. 7. Constellation diagram of synchronized BPSK received signal

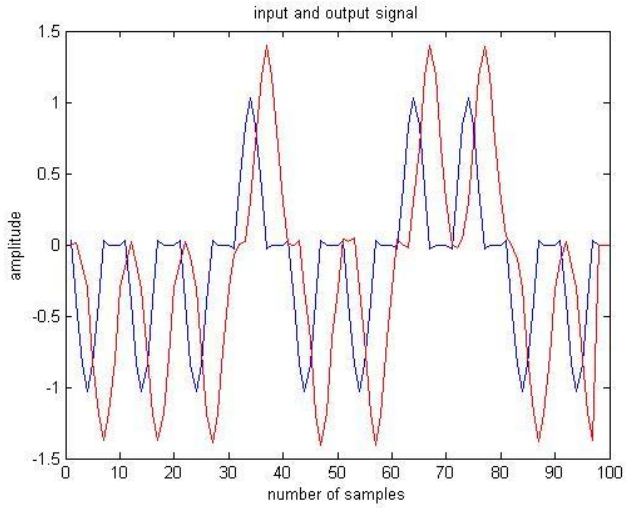

Fig. 8. Input and output plot

The costas loop is having disadvantages of long settling time and instability. The DPLL mechanism for frequency and phase estimation used here can overcome these problems. This scheme also overcomes the problem for recovering the signal with higher offsets.

To illustrate the mechanism of DPLL frequency and phase estimations are done. An input signal with a carrier frequency f_c of 6KHz and sampling frequency f_s of 20 kHz is used with different carrier offset. Fig. 9(a) shows the plot of frequency tracking using the DPLL frequency estimator. The phase estimator for phase tracking is given in Fig. 9(b).

Here frequency offset f_o of -1KHz and phase offset of 22.5° ($\pi/8$) is used. The output of frequency estimator with different value of μ which represents stability is given in Fig. 5. From Fig. 5 we can see that as value of μ varies the settling time also varies. For larger value of μ, the settling time is low, while for smaller vale of μ settling time is higher.

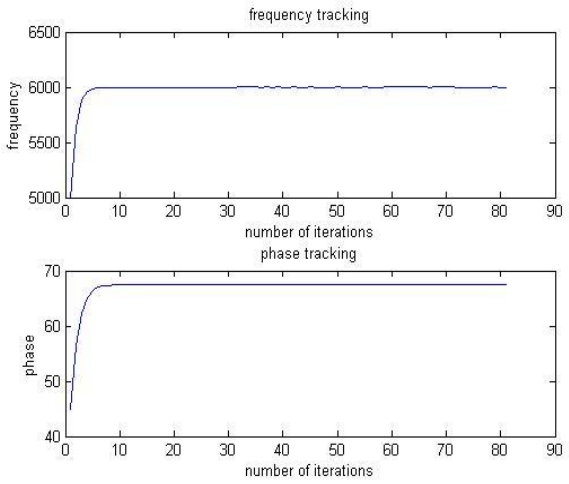

Fig. 9: (a) Frequency tracked by frequency estimator in DPLL. (b) Phase tracked by phase estimator in DPLL

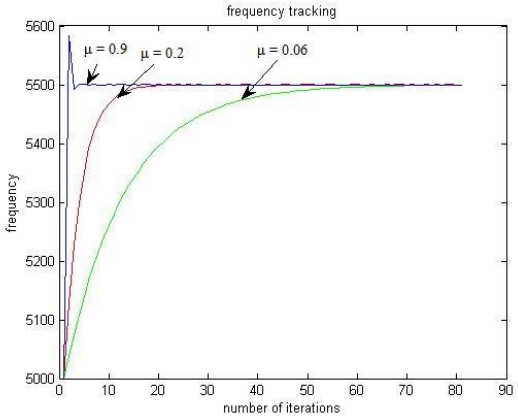

Fig. 10: Frequency tracked by frequency estimator in DPLL for different values of μ.

Hence the higher stability can be achieved by increasing the value of μ.

The comparison shows that DPLL is more stable with less settling time. It is faster and has wide range. The costas loop works for a lower offset in compared to DPLL and has a disadvantage of time delay.

V. CONCLUSION

Comparison of complete time domain simulations on Costas loop and DPLL synchronization mechanism is presented in this paper. The operation of both the tracking methods is presented here. The costas loop for carrier recovery is applicable only at lower carrier offset. This disadvantage can be overcome while using DPLL frequency and phase estimator.

DPLL frequency and phase estimator is having a low settling time in compared to Costas loop and hence is more stable.

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