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A Comparative Analysis InP/InGaAs δ Doped based NPN and PNP HBT

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***Abstract*—In this paper, a comparative study of InP/InGaAs δ doped based npn and pnp HBT is presented using two dimensional (2D) simulation TCAD Silvaco tool. The models are tuned for proper validation with experimental results in 2D simulation environment. The DC, AC and RF of both the devices have performed and compared on the basis of same physical geometry. For npn HBT a maximum of current gain beta (β) 254, f_{max}=14.34 GHz, BV_{CEO}=2.72V, and $V_{CE,\ offset}$=20mV where as for pnp HBT a maximum of current gain beta (β) =50 V, f_{max}=1.8 GHz, $BV_{CEO=}$-7.5V, and $V_{CE,Offset}$=-0.18V has achieved. The above comparison is also including the effect of spacer and delta doping in the performances of high frequency applications.**

Keywords*—InP/InGaAs, NPN and PNP Heterojunction bipolar transistors

I. INTRODUCTION

InP based HBT are among the highest performance III-V semiconductor device to date and are mostly suitable for high speed ICs, wide bandwidth analog, digital and RF application due to its excellent material properties. This type of HBT has several advantages such as large valence band discontinuity, low turn on voltage and compatible with a device having long wavelength and can operate in THz range [1, 2]. In an HBT higher emitter injection efficiency is due to band gap difference and it is important that a significant amount of band gap difference falls across the valence band in case of npn InP/InGaAs HBT. However, in case of pnp, conduction band alignment is suitable to reduce the electron injection into the emitter while a small value of valence band discontinuity help hole injection from the emitter into the base [3]. Composition grading across the depletion region of Emitter-Base junction is usually carried out to reduce the potential spike, but grading is difficult to precisely control and is not applicable to InP/InGaAs HBT [4]. Thus by reducing the potential spike we can lower the turn on voltage which is necessary to reduce the power consumption [1].In this paper potential barrier is lowered by using a thin sheet of charged layer in both npn and pnp HBT known as δ-doped layer. This layer is placed in between the two spacer layer, because as it is moved towards the hetero-interface, the effect of barrier lowering increases [5]. Hence the δ-doping is used in npn to increase the hole barrier whereas in pnp to increase the electron barrier. The thin spacer layer in between base and emitter layer reduces the charge storage, thus increases the current gain. However a thicker spacer is undesirable as it increases the electron base transit time which is undesirable for the design of microwave transistor [5]. By using the δ-doped layer offset voltage is reduced and minimization of offset voltage is important for InP/InGaAs HBT because the breakdown voltage of these HBT is very low [5]. The offset voltage is completely eliminated by matching the turn on voltage of the two junctions. . So, in this paper; The device is properly modelled and validated with the fabrication result of the reference papers for npn HBT [6], for pnp HBT [7].As model is validated for both npn as well as pnp HBT , the DC,AC, and RF characteristics are extracted and compared between them. The detailed device structure of npn HBT and pnp HBT is presented in Section 2, theoretical formulations and model developed is presented in Section 3. Results and Discussions are presented in Section 4 and the paper is finally concluded in Section 5.

II. DEVICE STRUCTURE

The studied InP/InGaAs δ doped npn HBT consisted of a 1.5μm undoped and linearly graded $In_xGa_{1-x}P$ (x: 0.52→1) buffer layer, a 0.15 μm undoped InP layer, a 0.35 μm $n^+=1\times10^{19}$ cm^{-3} $In_{0.53}$ $Ga_{0.47}As$ subcollector layer, a 0.5 μm $n^-=5\times10^{16}$ cm^{-3} $In_{0.53}$ $Ga_{0.47}As$ collector layer, a 0.1 μm $p^+=1\times10^{19}$ cm^{-3} $In_{0.53}$ $Ga_{0.47}As$ base layer, a 50 Å i-$In_{0.53}$ $Ga_{0.47}As$ spacer layer, a $n^+=2\times10^{12}$ cm^{-2} δ-doped sheet, a 50 Å i-$In_{0.53}$ $Ga_{0.47}As$ spacer layer, a 0.1 μm $n=5\times10^{17}$ cm^{-3} InP emitter layer, and a 0.3 μm $n^+=1\times10^{19}$ cm^{-3} $In_{0.53}$ $Ga_{0.47}As$ cap layer. The studied InP/InGaAs δ doped pnp HBT consisted of a 0.5 μm $p^+=1$ x $10^{19}cm^{-3}$ $In_{0.53}$ $Ga_{0.47}As$ subcollector layer , a 0.5 μm p^- = 5 x $10^{16}cm^{-3}$ $In_{0.53}$ $Ga_{0.47}As$ collector layer, a 500 Å n^+= 5 x 10^{18} cm^{-3} $In_{0.53}$ $Ga_{0.47}As$ base layer, a 50 Å i-$In_{0.53}$ $Ga_{0.47}As$ spacer layer, a p^+= 2 x $10^{12}cm^{-2}$ δ doped sheet, a 50 Å i- $In_{0.53}$ $Ga_{0.47}As$ spacer layer, a 0.1 μm p = 5 x 10^{17} cm^{-3} InP emitter layer, and a 0.3 μm p^+= 1 x10^{19} cm^{-3} $In_{0.53}$

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$Ga_{0.47}As$ cap layer. The structure of npn and pnp HBTs are presented in Fig.1 and Fig.2 respectively.

Use of InGaP buffer in the npn HBT device offers excellent thermal properties, thus a smaller thermal resistance. Each layer performs a specific function and the functional relationship between the layers decides the current gain and speed the device. The semi-insulating substrates have a low dislocation density, which is the key requirement for high speed circuit. Emitter cap layer is added for both cases on top of the emitter to minimize emitter ohmic contact resistance. The emitter, base, collector and subcollector areas of both npn and pnp transistors are $A_{Emitter}= 5\times10^{-5}$ cm^2,$A_{Base}=15.9\times10^{-5}$ cm^2, and $A_{Collector}=30\times10^{-5}cm^2$ respectively. The asymmetry of the emitter-base and collector-base junctions introduces an offset voltage. The offset voltage is an undesirable feature since it causes extra power consumption and reduced logic swing under active transistor operation [1] .large offset voltages would be expected due to a difference in turn-on voltage between the emitter-base heterojunction and base-collector homojunction. Smaller turn on voltage between the two junction leads to smaller collector emitter offset voltage. The dipole doping at the InGaAs/InP interface narrows the barrier to the point that electrons should be able to tunnel through the top part of it. In a single heterojunction bipolar transistor (SHBT), there is an energy spike in the emitter side which limits the electron transport from the emitter to the base and results in a higher turn on voltage of the emitter heterojunction. Therefore, elimination of this energy spike from the current transport would reduce the offset voltage significantly. Composition grading in the emitter junction can smooth out this energy spike and thus reduce the emitter turn-on voltage to that of the collector junction. A thicker spacer is not necessary because the effective base width, which includes the spacer thickness in this case, would produce a large electron base transit time which is not desirable in the design of the microwave bipolar transistors. This offset voltage is undesirable in the low bias integrated circuit applications, since it causes increased power dissipation and reduced output voltage swing. It is known that the offset voltage is attributable to the energy spike existing at the conduction band of the emitter junction and is equal to the difference between the turn-on voltages of the emitter and collector junctions.

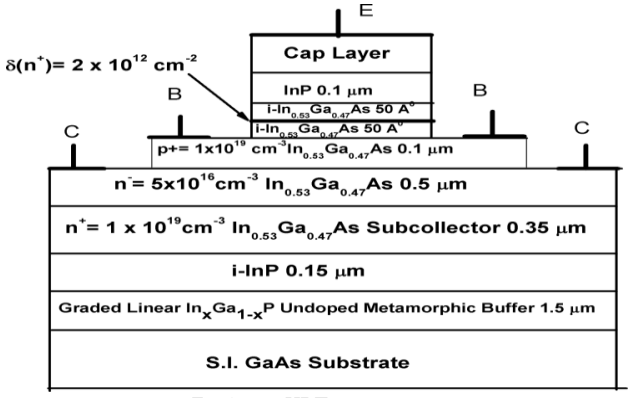

Fig 1: npn HBT structure

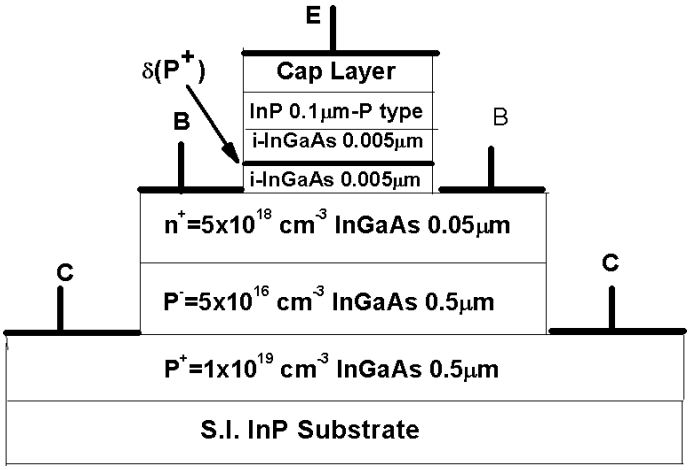

Fig 2: pnp HBT structure

III. MODEL SELECTION

In the simulation of the device structure various device model are tunned to get the desired result. Parallel Electric Field Dependence MODEL (FLDMOB) is required to model any type of velocity saturation effect. When parallel electric field dependence are used with energy balance the electric field term is replaced by a function of carrier temperature. FLDMOB should always be specified unless one of the inversion layer mobility models (which incorporate their own dependence on the parallel field) is specified. Bandgap Narrowing- Important in heavily doped regions. This model (BGN) is necessary to correctly model the bipolar Current gain. Auger -Important at high current densities. Auger recombination occurs through a three particle transition whereby a mobile carrier is either captured or emitted. Auger recombination accounting for high level injection effects. AUGER specifies that Auger recombination rate is probed. Concentration Dependent CONMOB- it specifies the concentration dependent mobility. Specifies that doping concentration dependent model to be used for electrons. Shockley-Read-Hall SRH Used to fixed minority carrier lifetime. To simulate the device in breakdown HBT requires selberherr impact ionization (selb) model. It is a temperature dependent parameter. For convergences purpose of absolute current and relative current ir.tol and ix.tol are selected during simulation respectively.

IV. RESULTS AND DISCUSSION

For the InP/InGaAs δ doped npn and pnp HBTs, DC, AC, and RF characteristic are obtained and the results are presented in this section. The gummel plot of both the HBTs is shown in Fig.3 and Fig.4 respectively, which is agreed with the reported fabricated result. The closely agreement of the results shows our accuracy of models. The DC current gain β (beta) for npn and pnp HBT are shown in Fig.5 and Fig.6 respectively. For npn HBT the maximum β is 254 where as in pnp HBT the maximum β is 50. The reason for high gain in npn HBT compared to pnp HBT is due to less number of minority carriers are injected back to the emitter.

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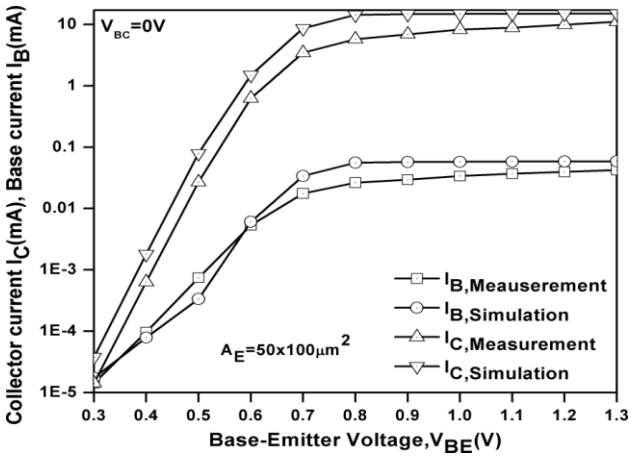

Fig 3:npn gummel plot match with experimental reference [6]

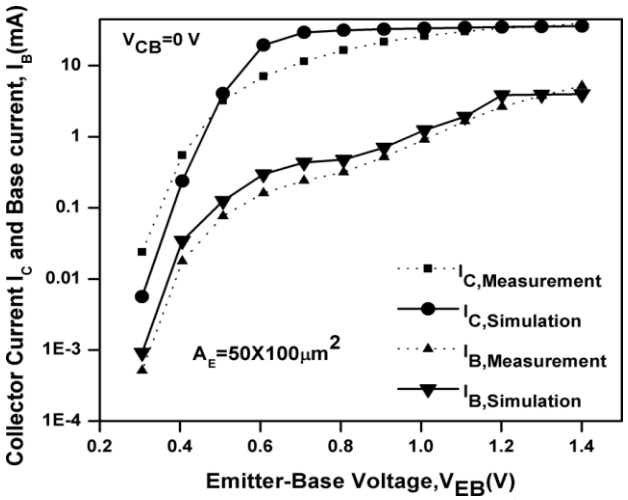

Fig 4:pnp gummel plot match with experimental reference [7]

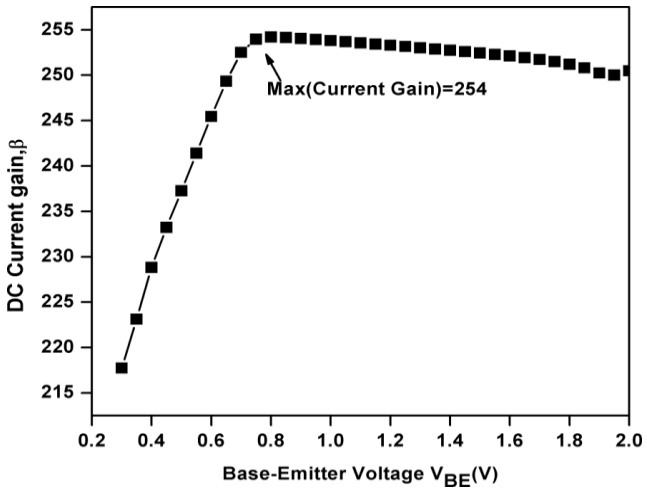

Fig 5: DC current gain (β) of npn HBT

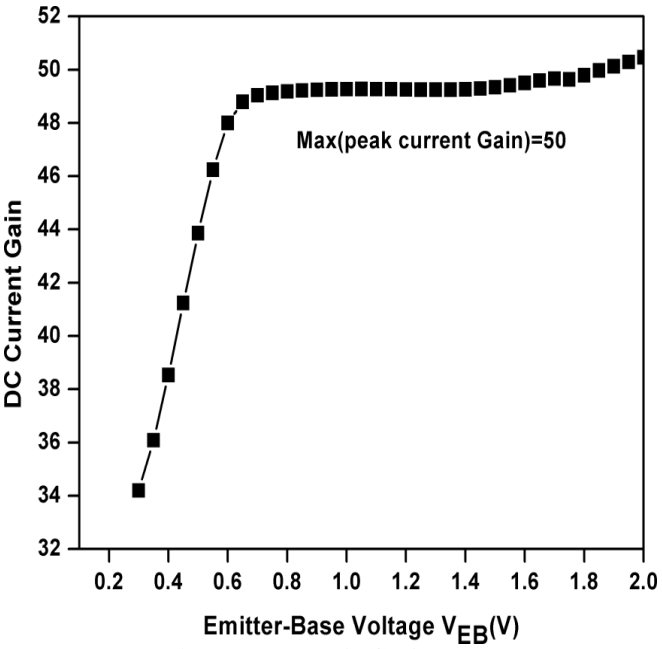

Fig 6: DC current gain (β) of pnp HBT

The I_C versus V_{CE} curves are shown in Fig.7 and Fig.8 for npn HBT and pnp HBT respectively. Due to convergence problem both have simulated with different base currents. Since for comparison purpose both have included at a common I_B=10μA. It is clear that for the same base current npn based HBT provides more collector current than the pnp based HBT. Such observation is evident in view of the highest β of npn HBT.

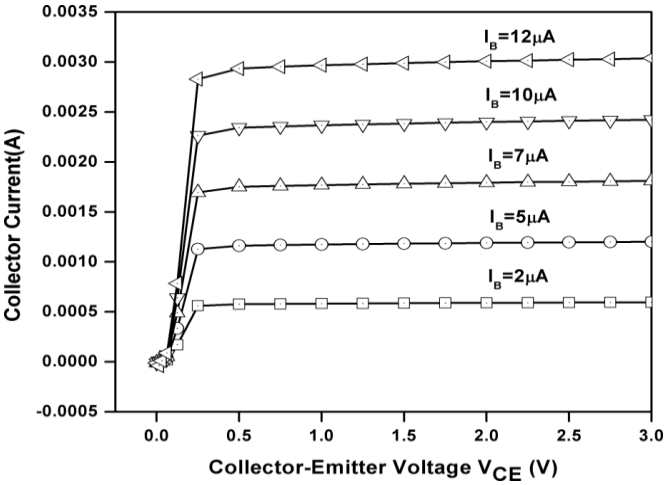

Fig 7: Output characteristics, V_{CE} vs I_C for npn HBT

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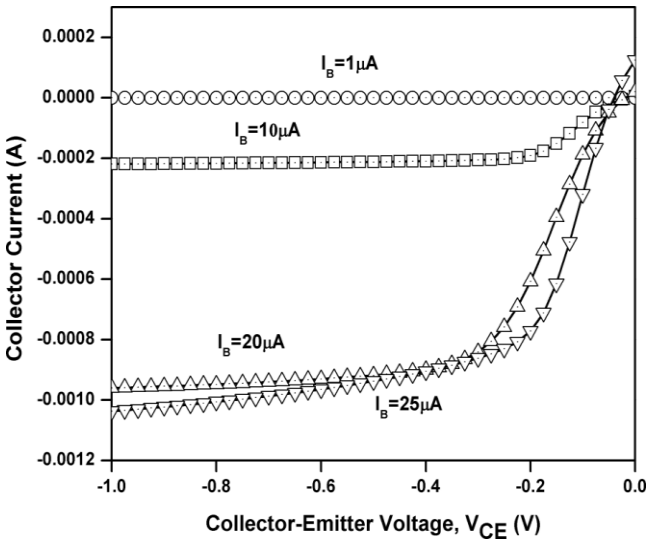

Fig 8: Output characteristics, V_{CE} vs I_C for pnp HBT

The Early voltage (V_A) is computed from backward extrapolated V_{CE}-I_C characteristics shown in Fig.7 and Fig.8 respectively. The observed Early voltages for npn and pnp HBTs are -42 V and 7.69 V respectively. The V_A is the important parameter to measure the output conductance. Higher V_A is desirable for a HBT for better circuit operation. The V_A can be expressed as [8]

$$V_A = \frac{\int_0^{W_B} N_{aB}(x)\,dx}{N_{aB}W_B\{\frac{\partial W_B}{\partial V_{CB}}\}} = \frac{Q_B(0)}{C_{CB}} \quad (1)$$

where $Q_B(0)$ is the total base charge at V_{CB}=0 V and C_{CB} is the collector base depletion capacitance.

The breakdown voltages in the open base configuration, BV_{CEO} for npn and pnp HBTs are shown in Fig.9 and Fig.10 respectively. The two HBTs are simulated at a base current of, I_B=1e-10 A. The reason for choosing such a small base current is to assume that the base terminal is open. The observed breakdown voltages for the HBTs are 2.75 V and -7.5 V for npn and pnp HBTs respectively. The open base configuration BV_{CEO} can be expressed as [9]

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \quad (2)$$

where BV_{CBO} is the CB breakdown voltage with the emitter left open. The low breakdown voltage for npn HBT can be understood from expression (2), that the high dc current gain of the device is mainly responsible for the same.

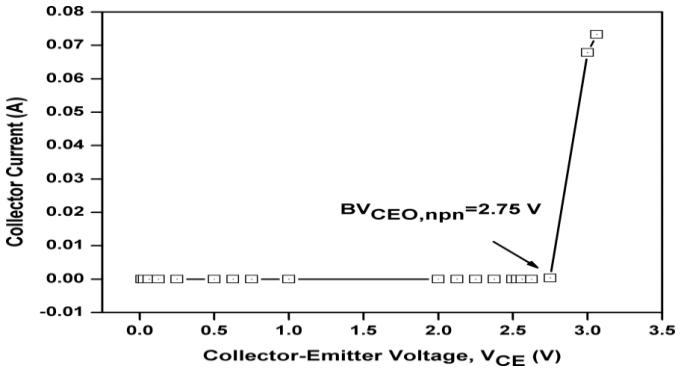

Fig 9: Breakdown voltage (V) of npn HBT

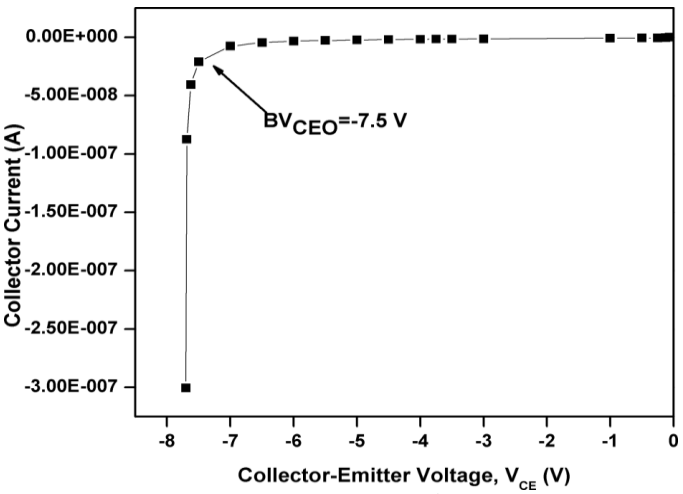

Fig 10: Breakdown voltage (V) of pnp HBT

The high frequency performance of the simulated HBTs are characterized by 'S' parameters extracted from the Silvaco tool. The cutoff frequency (f_t), defined as the frequency at which the magnitude of short circuit current gain $|h_{21}|=1$, is plotted in Fig. 11. They are recorded to be 30.1 MHz and 5.49 MHz for npn and pnp HBTS respectively. The cut-off frequency (f_t) can be expressed as

$$f_t = \frac{1}{2\pi\tau_b} \quad (3)$$

where τ_b is the base transit time, defined as the time required to discharge the excess minority carriers in the base through the collector current [10]

$$\tau_b = \frac{W_B^{\,2}}{D_{nB}} \quad (4)$$

where, W_B^2 is the width of base region, D_{nB} is the diffusion coefficient of carrier in the base region. The D_n value of electron is higher than that of hole [11]. Thus it is clear that npn HBT having lower τ_b than that of pnp HBT. Hence higher f_t is observed in the npn HBT .

f_{max} is the maximum oscillation frequency of a device and it is determined with the condition Massion's Unilateral Power Gain, $|MUG|=1$, using unit-gain-point method. The fmax of the both HBTs are presented in Fig 11.. The f_{max} of pnp and npn HBTs are found to be 1.97 GHz and

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14.84 GHz respectively. The maximum oscillation frequency is expressed as [10]

$$f_{\max} = \sqrt{\frac{f_t}{8\pi r_b c_{jc}}} \quad (5)$$

where f_t is cut-off frequency, r_b the base resistance, and c_{jc} is the collector junction capacitance.

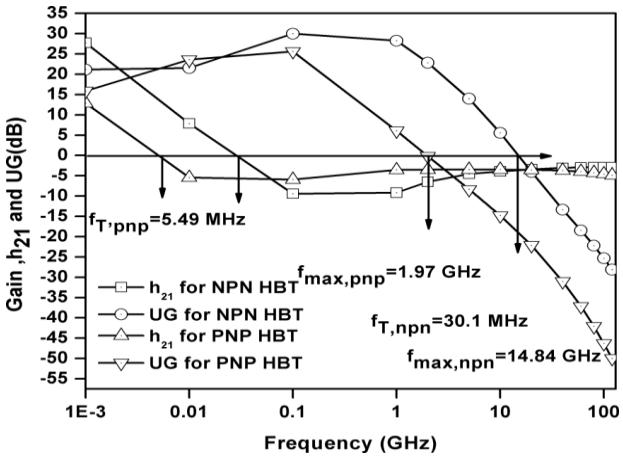

Fig 11: f_T, f_{max} of both the HBTs

The stability factor, K, measures whether a transistor will be unconditionally stable for arbitrary passive loads [12]. The Rollett stability factor can be expressed in terms of S-parameters as [10]:

$$K = \frac{1-|s_{11}|^2-|s_{22}|^2+|\Delta s|^2}{2|s_{12}.s_{21}|} \quad (6)$$

where $\Delta s = s_{11}s_{22} - s_{12}s_{21}$. The stability factors of all the transistors are shown in Fig 12. It is observed that the stability issue of pnp HBT is better than the npn HBT as K >1.

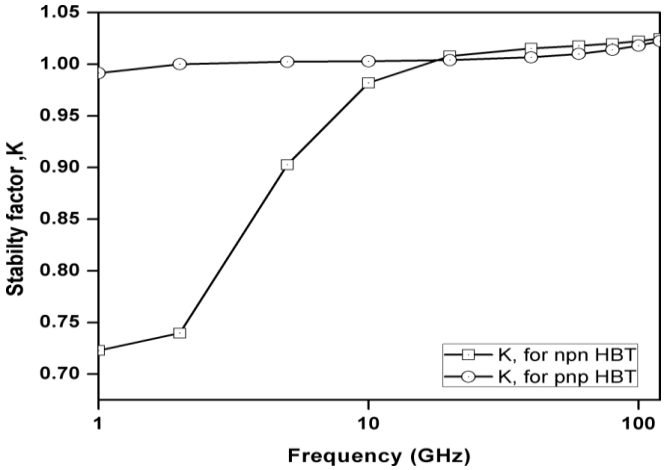

Fig 12: Stability factor, K of both the HBT

V. CONCLUSIONS

InP technology is preferred over other technologies for high linearity low noise power amplifiers because of their higher integration, higher frequency, higher power, higher power efficiency, lower noise, and lower cost. The future is bright for structures and devices based on InP material system because of their higher integration. In the present work we use Silvaco TCAD 2D Simulator to extract the various value of device parameter. The estimated value of the current gain in this paper agrees well with the measured value reported by fabrication. HBT based on InP/InGaAs are attractive for optical and high speed application because of high electron mobility in the base region. In addition the substrate has higher thermal conductivity and lower surface recombination velocity. At the same time InP buffer is advantageous in reducing thermal resistance. Excellent current gain and high frequency of operation makes the InP based HBT a popular candidate for hand-held wireless area. In addition low turn-on voltage consequently makes the device highly preferable for low power application. Addition of spacer and δ-doped layer lowers the offset voltage while increasing the gain. Better performance provides a great promise to the device for high speed and low power application. Moreover the most extensive FOM analysis for these devices such as current gain, I-V behavior, maximum cutoff frequency and breakdown voltage for these devices have been carried out. From the various figure of merits we can easily find that npn HBT exhibit better performances as compared to pnp HBT.

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