

A Compact Power Amplifier Design for RF Receiver

I. Dhurgabai,
Assistant Professor,
Department of ECE
Theni Kammavar Sangam College Of Technology

K. Sreevenkatesh
Assistant Professor,
Department of ECE
Sacs Mavmm Engineering College

Abstract— The rf power amplifier is the main component in rf receiver to make detection efficient. The design is focused on the size reduction of the power amplifier. The power amplifier is designed to operate at 12GHz frequency. The size reduction technique chosen is fractal technology. Fractal technology applied is to squeeze the distributed elements used in amplifier design.

Keywords—:fractal technology,squeezing transmission line, k - Δ test

I. INTRODUCTION

Power amplifier is the important component for large signal amplifications. The main aim is to design power amplifier by squeezed transmission line coupler for the desired operating frequency. The main components in design are power divider, Matching networks, dc biasing network, unconditionally stable transistor as amplifier in two stage to increase power gain and power combiner.

II. DESIGN PROCEDURE

The transistor selection for power amplifier is the first step in design procedure. The operating frequency selected is 2GHz. For the operating frequency the transistor behavior is analysed in ads with proper dc biasing. The dc biasing network is designed for the chosen transistor specification. The dc biasing network is created by lumped elements which include R, L, C and voltage biasing dc source. Based on design formulation the values are determined. The biased transistor is analysed by determining its s-parameters. From s parameter values the stability of transistor is analysed by $k-\Delta$ test. If stability criteria is satisfied transistor selection sounds better for amplification. Then based on s-parameter input and output matching T network is designed. The lumped element values of matching network are identified from smith chart by plotting s_{11} and s_{22} . By plotting s_{11} input matching network shunt C and shunt L are calculated. Then by plotting s_{22} input matching network shunt C and shunt L are calculated. Then the modified transistor network acts as single stage power amplifier.

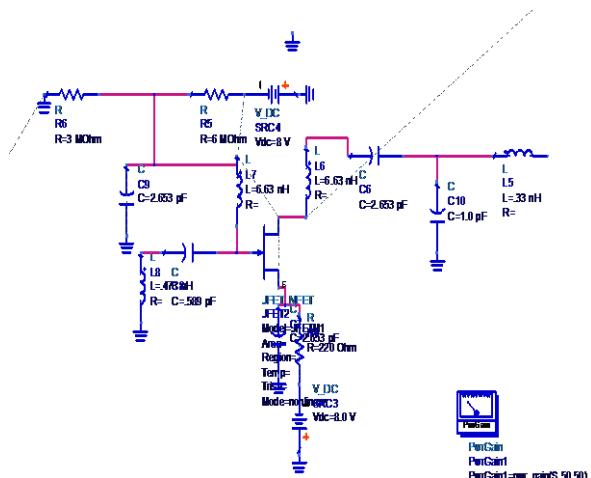


Fig S parameter modified transistor structure

Then two single stage power amplifier forms dual stage power amplifier. The input power is splitted using a power divider and feeds both the single stage amplifier structure. The power divider used here in our proposed structure is squeezed branch line coupler. The squeezing or fractal strategy is adopted to make the structure compact which suits the modern electronic devices.

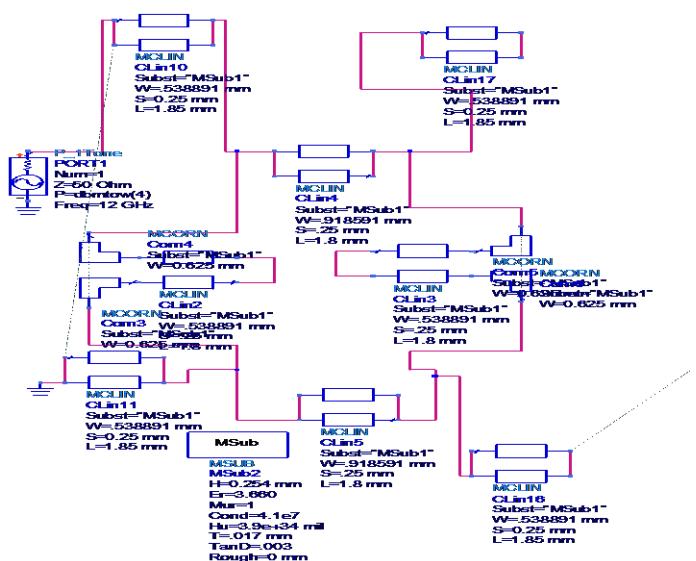


Fig squeezed transmission line power splitter/Combiner

The squeezed coupler in two stage power amplifier design makes the design compact by reducing length and width providing the same response. The squeezed structure length is reduced to 13.5 mm from 38.11mm. The structure is simulated in ADS and the result is analysed by plotting the return loss and power gain for the conventional structure and modified structure.

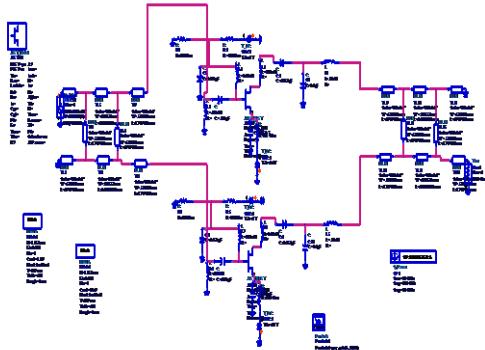


Fig conventional branch line coupler power amplifier schematic



Fig conventional branch line coupler power amplifier layout

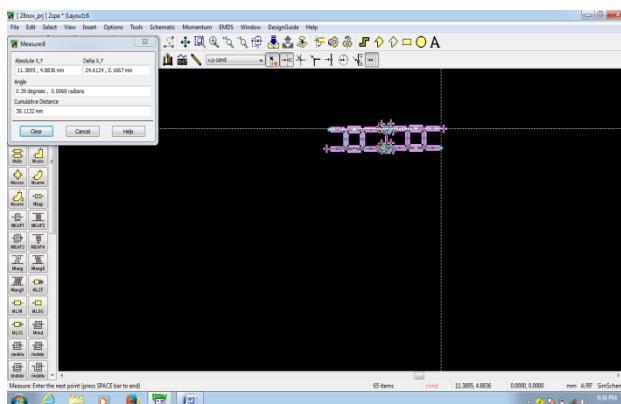


Fig conventional branch line coupler power amplifier size measurement in ads

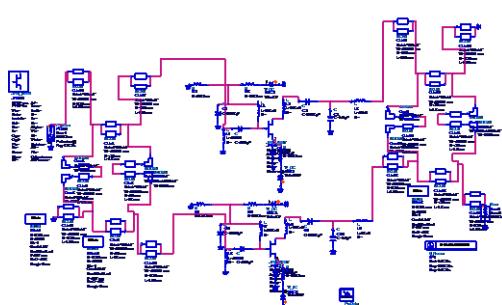


Fig squeezed line coupler power amplifier schematic

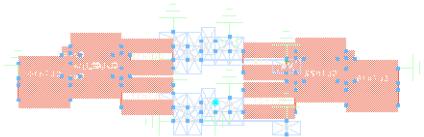


Fig squeezed line coupler power amplifier layout

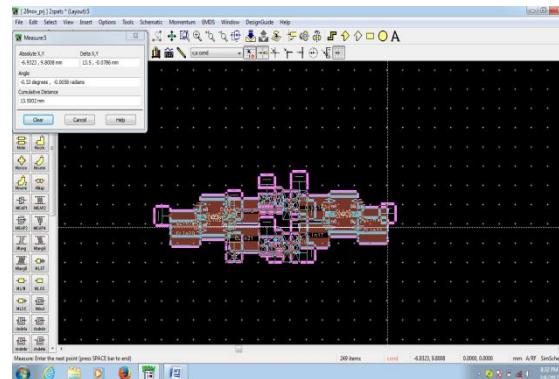


Fig squeezed line coupler power amplifier size measurement in ADS

III. SIMULATION RESULTS

The design is simulated using ads. The transmission line length and width used for design are calculated in lincalc of ads by specifying material properties, operating frequency and arm impedance. The S parameters simulated are shown below. The return loss is obtained less at 2 GHz frequency and power gain is better at 2GHz frequency even when transmission line used is squeezed in design to reduce size

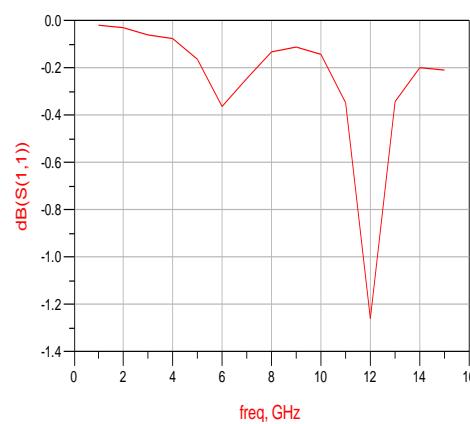


Fig Return loss vs frequency plot

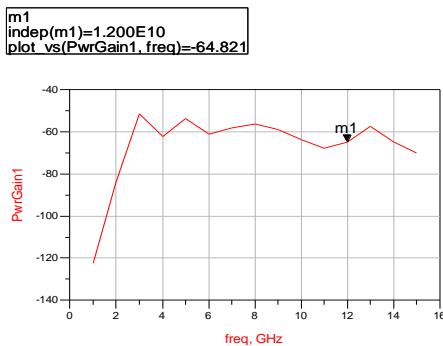


Fig power gain vs frequency

IV. CONCLUSION

The rf power amplifier is the main component in rf receiver to increase signal strength. the boosted signal strength makes detection sound better. the component size is one of the design constraint. the size is reduced by fractal technology when the lumped elements are replaced by distributed elements. the modified design produces same response even when size shrinks which suits the modern electronics technology. the size could be reduced by more squeezing and converting dc biasing network and matching network with distributed elements. The replaced elements could be further squeezed to make component compact.

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