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A 10µW Hybrid OTA with Bulk-Biasing driving 20nF capacitive load with 115dB DC-gain and 1.68MHz GBW

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***Abstract*—For better area and power efficient, single stage amplifiers are a better replacement of their multi-stage cmplifies ounterparts, particularly for display applications that imply massive buffer amplifier in their column drivers. This paper employs a signal-current enhancer technique for a single-stage amplifier to achieve significant enhancement of DC gain, gain-bandwidth product (GBW) and slew-rate. Ana bulk-biasing technique employed to minimize the internal node capacitances and area of OTA. Analytical treatments of the signal-current enhancer technique in terms of performance limits and robustness reveals that hybrid OTA can suppress the fundamental power-efficiency limit set by the basic differential-pair amplifier. The proposed hybrid OTA is implemented in a standard PTM 65 nm CMOS technology. Working under a 0.5V supply and proven by simulation results, the resultant OTA when driving an output capacitor of 20nF attained 115 dB DC gain, a GBW of 1.68 MHz and an Slewrate of 0.15 V/µs, consuming only 10µw of current and requiring no compensation capacitor.**

***Keywords*—Amplifier, frequency response, large capacitive loads, transient response, signal- current enhancement .**

I. INTRODUCTION

For many modern applications require high-gain and fast-settling operational transconductance amplifiers (OTAs) driving off-chip loads in the order of hundreds (or even thousands) pico farads, such as high accuracy modulators, analog-to-digital converters, low-dropout regulators, headphone drivers and display applications like wide-dimension low-temperature polysilicon (LTPS) LCD panels [1] that involve thousands of buffer amplifiers in their column drivers, the area and power budgets of each buffer amplifier are extremely tight to meet the market pressure on cost and display quality [1]. The buffer amplifiers should drive a wide range of capacitive load (C_L) up to tens of nano-farad (nF), while securing adequately large DC and output swing. Battery-operated portable systems integrate most of these blocks and, in addition, they work under tight power and area budgets.

In this context the design of high-gain OTAs driving heavy capacitive loads is a challenging task, especially when nanometers technologies are adopted, as they suffer from a drastic reduction of the intrinsic gain that can be only partially mitigated by the adoption of non-minimum channel length transistors. In principle, stacked-device (i.e., cascode) topologies provide high DC gains but they reduce the output swing and have been progressively abandoned for this reason. Presently, the only viable solution to get DC gains in excess of 80 dB in scaled technologies is the adoption of multistage architectures, where simple gain stages are exploited. Since they provide very high DC gains without sacrificing output swings. Of course, the simplest gain stage available is a common source amplifier entailing only two complementary MOS transistors between the supply rails, though this choice limits the number of topologies available to the designer. However, the need for frequency compensation increases their design complexity, which also restricts their drivability of (range and size), area and power efficiencies.

The design of multistage amplifiers is also complicated by the increased number of high impedance nodes (and, in turn, of low frequency poles and zeros in the loop-gain transfer function) which compromise stability, especially when the capacitive load is heavy. An OTA consuming power in µW-range generates tiny signal currents by input differential pair. By effectively enhancing these signal currents, both the GBW and gain can be significantly improved. This paper presents a signal-current enhancer to enhance the magnitude of the signal currents generated by the input differential pair. The signal-current enhancer is able to augment both the voltage gain and GBW even when non cascode structure is engaged.

II. OPERATIONAL TRANSCONDUCTNACE AMPLFIER WITH SIGNAL-CURRENT ENAHCNER.

In this section, the basic operation of the signal-current enhancer circuit with bulk biasing is described for OTA design.

A. Concept of Signal-Current Enhancer

The signal current enhancer circuit as shown in Fig. 1. In circuit I_B indicates the DC bias current and is shows small signal current generated from input differential amplifier. This cell consumes a current of $2(k+1)I_B$. The OTA was designed for driving a large capacitive load by cascading of signal-current enhancers. The bulk terminal PMOS transistor can access directly without effecting other device performance. The minimum supply voltage require for each enhance circuit is $V_{GS}+V_{DS(sat)}$. With bulk biasing of PMOS gate-to- source voltage can be reduced for the same value of current. Which is useful to design amplifier with low-supply voltage (< 1 V).

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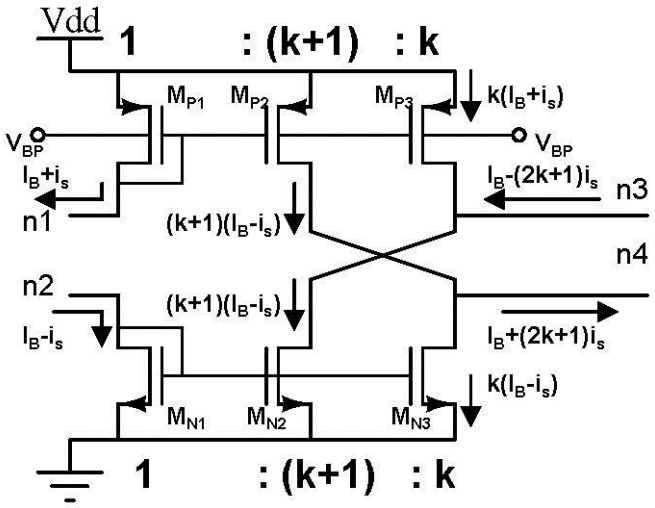

Fig. 1 Signal-current enhancer with bulk biasing – indicated with dc and small signal currents

Here, six signal-current enhanced cascaded to achieve high gain and to drive capacitive loads. The arrangement of cells are shown Fig. 2. The dc and signal current at the output of Cell 2 are I_B and $\pm(2k+1)^2 i_s$, respectively. Similarly, the dc and signal currents at the output of Cell 6 become I_B and $\pm(2k+1)^6 i_s$ respectively. The dc ration, signal gain, and supply current (I_{DD}) of the six cascade structures are, therefore, given by

$$\text{dc ratio} = \frac{I_{BOUT}}{I_{BIN}} = \frac{I_B}{I_B} = 1 \tag{1}$$

$$\text{signal gain} = \frac{(2k+1)^6 i_s}{i_s} = (2k+1)^6 \tag{2}$$

$$I_{DD} = 6\left[2(k+1)I_B\right] \tag{3}$$

The proposed design uses less supply current, voltage and because of bulk bias less parasitic poles generated by signal nodes. Since for the bias current I_B PMOS require small geometrics. In principle, the maximum achievable bandwidth of the proposed amplifier is higher due to less parasitic effects.

B. Small-Signal Analysis of OTA with Signal-Current Enhancers

In Fig. 3, the cascade signal-current enhancer is applied to a classical OTA by inserting it between the input differential pair and the output stage. When an input differential signal v_{in} is applied to the input stage $i_s=0.5g_{m1}v_{in}$ where g_{m1} is the transconductance of M_1 is generated, and i_s is further enhanced by the signal-current enhancer by $(2k+1)^6$ times. The signal current is additionally scaled up by the transistor size ratio (i.e m) of the current mirrors to generate an output signal current i_o of $m(2k+1)^6 g_{m1}v_{in}$. The enhanced i_o will be used to charge/discharge C_L according to the change of v_{in} so that the GBW is also widened by $m(2k+1)^6$ times to yield

$$GBW = m(2k+1)^6\left(\frac{g_{m1}}{C_L}\right) \tag{4}$$

The voltage gain likewise boosted by $m(2k+1)^6$ time to give

$$\frac{v_{out}}{v_{in}} = m(2k+1)^6 g_{m1}\left(r_{No2} // r_{Po2}\right) \tag{5}$$

Where r_{No2} and r_{Po2} are the rain resistance of M_{No2} and M_{Po2}, respectively. The total current I_{DD} of the proposed OTA is hence

$$I_{DD} = \left\{6\left[2(k+1)\right]+m+4\right\} I_B \tag{6}$$

C. Largel-Signal Analysis of OTA with Signal-Current Enhancers

The large signal operation of the signal-current enhance is shown in Fig. 4. Two different cases are considered: having $2I_B$ at one input and 0 current at other, and vice versa. It is noted that the output current of the enhancer are 0 and $2(k+1)I_B$, respectively.

The large-signal responses [i.e., the positive slewing (SR_+) and negative slewing (SR_-)] of the proposed OTA are shown in Fig. 5. When a rising step input is applied to Vip_+ , the tail current goes entirely to M_1 and so the input currents to Cell 1 are exactly the case shown in Fig. 4(a). The input currents $2I_B$ and 0 are processed by Cell 1 to be the output currents 0 and $2(k+1)I_B$. Based on the concepts presented in Fig. 4(a) and (b), after going through all the six cells, the output currents of the six cascade signal-current enhancers are $2(k+1)^6 I_B$ and 0, respectively. Since the input current of M_{N01} is 0, only M_{P01} and $M_{Po2}$are turned ON, and the current of $2(k+1)^6 I_B$ from Cell 6 is further scaled up by the m-ratio of M_{Po1} and M_{Po2}. The output transient current is thus $2m(k+1)^6 I_B$, and the SR_+ is also heightened by m(k+1)6 times as shown in Fig. 5(a), when comparing with a standard OTA. Similarly, as shown in Fig. 5(b), when a rising step input is applied to V_{in} the SR_- can also enjoy the same boosting factor. As such, the proposed circuit can enhance the transient current on its own, without SR enhancement circuit, to achieve

$$SR = m(k+1)^6\left(\frac{2I_B}{C_L}\right) \tag{7}$$

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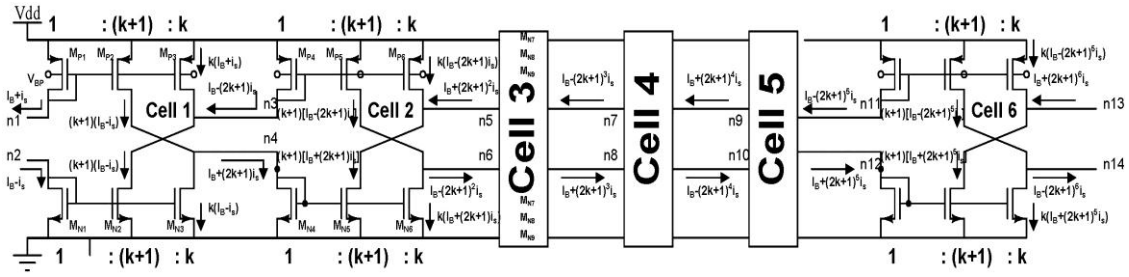

Fig. 2 Signal current enhancer (six cascade cells)- indicated both dc and signal currents

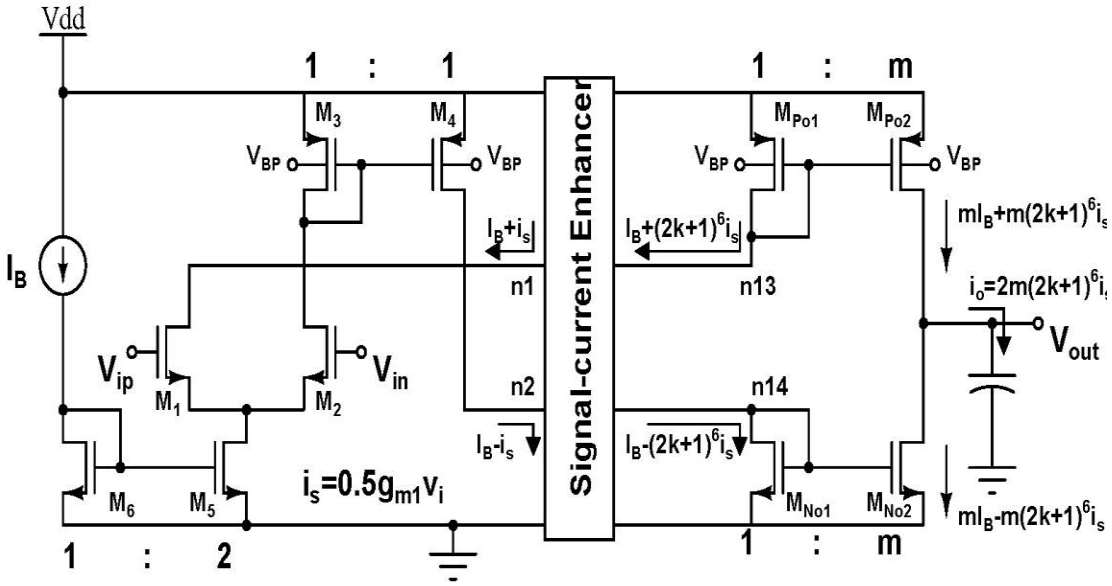

Fig. 3 Hybrid OTA with bulk biasing current-enhancer

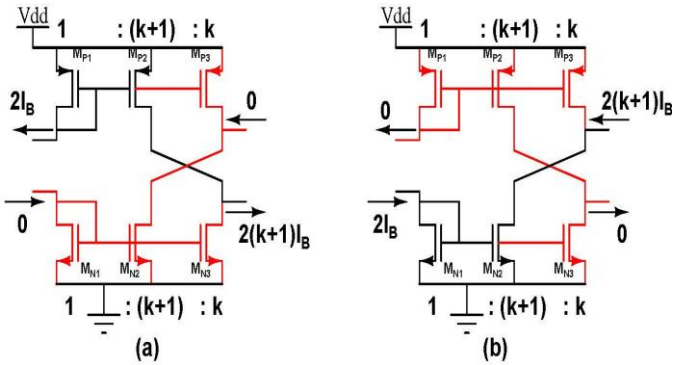

Fig. 4 Large-signal responses of signal-current enhancer (a) Case 1: input currents are $2I_B$ and 0. (b) Case 2: input current are 0 and $2I_B$

The node resistances, node capacitances, and estimated locations of parasitic poles at node n0-n14 can be tabulated, as shown in Table I. In order to locate tall parasitic poles beyond the GBW to achieve sufficient phase margin (PM), the values of k and m cannot be too large. Therefore, k=2 is selected to provide an improvement factor of $(2k+1)^6$ =15,625 for GBW and voltage gain, and to achieve an enhancement factor of $(k+1)^6$=729 for the slewrate. These improvements are sufficient to have the OTA outperform the state-of-art designs.

Table 1 Parasitic Poles in Hybrid OTA

Nodes	Node resistance	Node capacitance	Parasitic Poles
n1,n3,n5,n7,n9,and n11	$1/g_{mp}$	$(2k+2).C_{gp}$	$g_{mp}/(2k+2).C_{gp}$
n13	$1/g_{mp}$	$(m+1).C_{gp}$	$g_{mp}/(m+1).C_{gp}$
n0	$1/g_{mp}$	$2C_{gp}$	$g_{mp}/2C_{gp}$
n2,n4,n6,n8,and n12	$1/g_{mn}$	$(2k+2).C_{gn}$	$g_{mp}/(2k+2).C_{gn}$
n14	$1/g_{mn}$	$(m+1).C_{gn}$	$g_{mp}/(m+1).C_{gn}$

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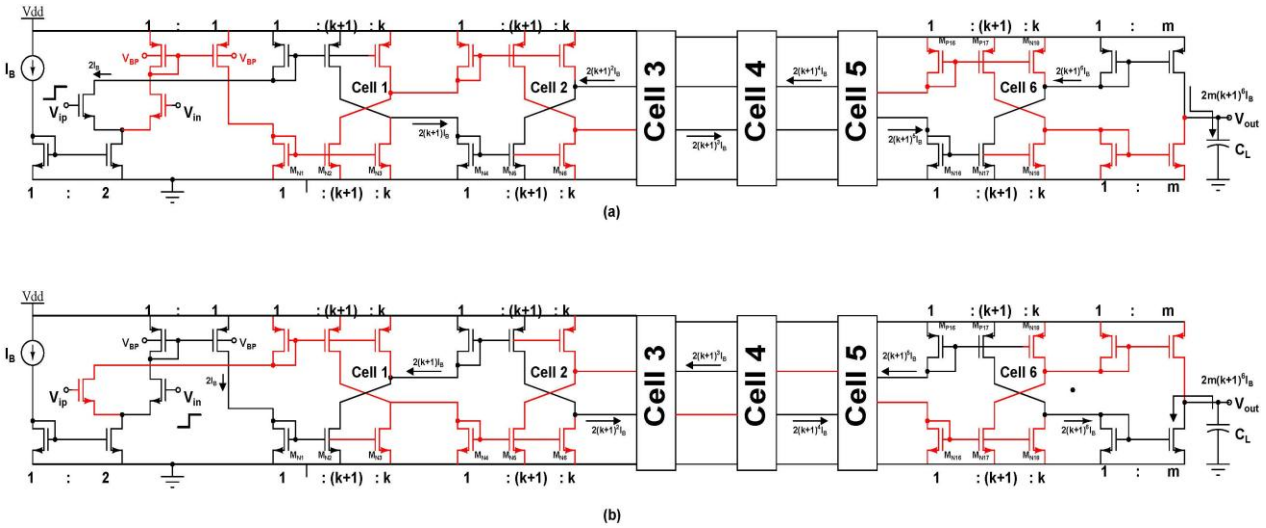

Fig. 5 Large-signal responses of hybrid OTA (a) rising step input at V_{ip} and (b) rising step input at V_{in}

A summary on the performance of OTA with signal-current enhancer is tabulated in Table 2. The supply current increases linearly with k and a factor of 6 due to the six cascade cells used. Providentially, the GBW, voltage gain, and SR are all exponentially increased by a power of 6, which augment all significantly at only a slight increase in power.

Table 2 Summary of Performances of Hybrid OTA

Supply current	$I_{DD}=\{6[2(K+1)]+m+4\}I_B$
GBW product	$GBW=m(2K+1)^6\times(gm1/C_o)$
Voltage gain	$V_O/V_{in}=m(2k=1)^6\times g_{m1}(rono2//r_{oPO2})$
Slew rate	$SR=m(k+1)^6\times(2I_B/C_O)$

III. SIMULATION RESULTS

Amplifier in Fig. 3 implemented in 65 nm PTM CMOS technology. This CMOS technology has a nominal supply voltage of 0.5 V. The gate-to-source voltage of the NMOS and PMOS transistor are 0.25 and -0.25 V. The threshold voltage of PMOS transistor with a bulk bias voltage of 0.25 V is 0.32 V. The unit size of NMOS transistor is 2.5 µm/0.5 µm and that of PMOS transistor is 4 µm/0 .2 µm. The selected values of k and m are 2 and 3. The proposed OTA does not require compensation capacitor. The simulation results with 0.5V supply voltage and 20nF load capacitance C_L are presented here.

Fig. 6 shows the simulation frequency responses of bulk-biased hybrid OTA. B The obtained GBWs and PMs are 1.68 MHz and 53^0 for C_L=20 nF, 0.877 MHz and 71^0 for C_L=40 nF, and 0.7 MHz and 74^0 for C_L=50 nF, respectively. Fig. 7 illustrate the frequency response of the OTA in unity-gain configuration. The low-impedance nodes (i.e., n0–n14) in the proposed signal-current enhancer have minute effects on the stability of the proposed OTA since the parasitic poles are located at much higher frequencies than the GBW. Fig. 8 depicts the transient responses of the proposed OTA in unity-gain configuration with a step input of 0.5 V. The average slewrates are 0.15 V/µs for C_L=20 nF, 0.075 V/µs for C_L=40 nF, and 0.06 V/µs for C_L=50 nF, respectively. The ovel all performance of realized amplifier is summarized in Table 3. The performance of the amplifier is compared with relevant design in Table 3.

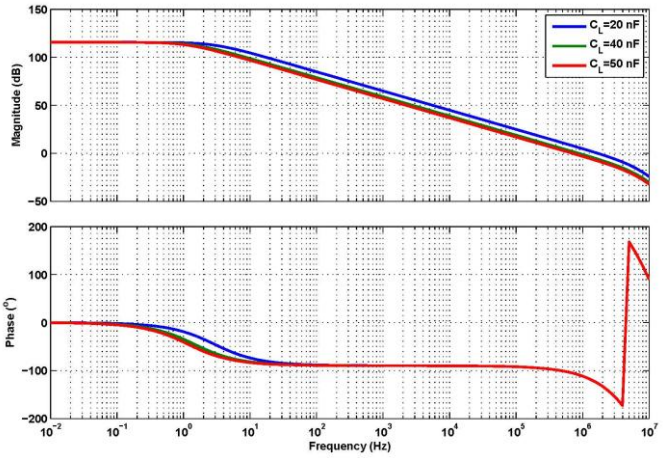

Fig. 6 Simulated open-loop frequency responses of bulk-biased Hybrid OTA

Generally, the efficiency of a frequency compensation scheme is characterized by four commonly used figures of merit (FOM).

$$FOM_s=\frac{GBW.C_L}{Power},\ IFOM_s=\frac{GBW.C_L}{I_{DD}}$$

$$FOM_L=\frac{SR.C_L}{Power},\quad IFOM_L=\frac{SR.C_L}{I_{DD}}$$

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Table 3 Performance Summary and Comparison

Parameters	IAC [2]	CFCC[3]	CBMC[4]	CLIA[5]	NCM[6]	Hybrid OTA[1]	This work
Technology(µm)	0.35	0.065	0.35	0.13	0.18	0.13	0.065
C_L (pF)	150	500	15 000	680	500	10 000	20 000
V_{DD} (V)	1.5	1.2	2	1.2	1.2	0.7	0.5
I_{DD} (µA)	20	17	72	10.5	3	24	10µw
Dc gain (dB)	110	>100	>100	>100	84	~100	115
GBW(MHz)	4.4	2	0.95	3.37	0.396	1.99	1.68
SR (V/µs)	1.8	0.65	0.22	0.67	0.0115	0.7	0.15
PM (°)	57	52	52.3	45	81.4	47	53
On-chip capacitance(pF)	1.6	1.15	2.6	0.587	0	0	0
FOM_S (MHz.pF/mW)	22 000	49 020	98 958	181 873	55 000	1 184 524	3 360 000
FOM_L (V/µs.pF/mW)	9000	15 931	22 917	36 159	1597	416 667	300 000
$IFOM_S$ (MHz.pF/mA)	33 000	58 823	197 916	218 247	66 000	829 166	1 680 000
$IFOM_L$ (V/µs.pF/mA)	13 500	19 118	45 834	43 391	1916	291 667	150 000

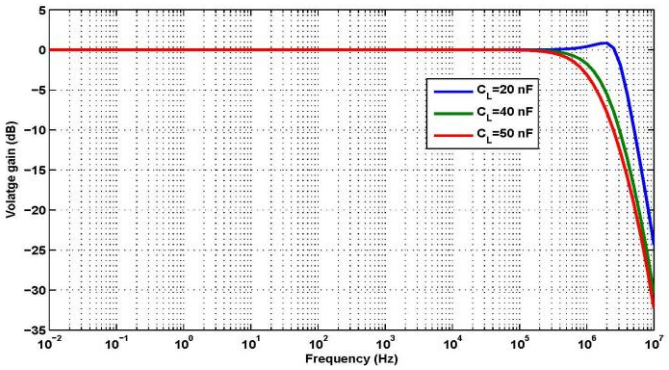

Fig. 7 Simulated frequency responses of bulk-biased Hybrid OTA in unity-gain configuration.

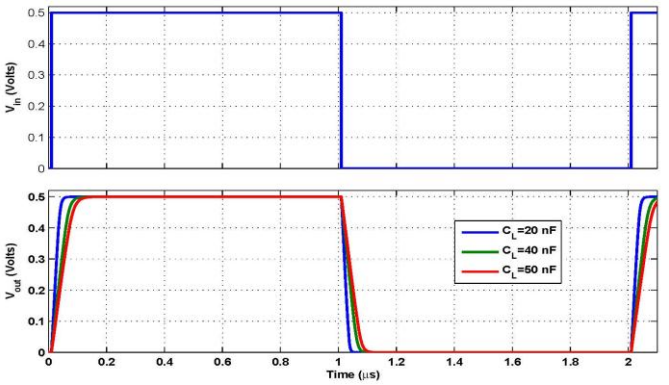

Fig. 8 Step responses of Hybrid OTA

FOM_S and FOM_L evaluate the compensation performance on a system level design point of view, while $IFOM_S$ and $IFOM_L$ address an inspection on the transistor level, since both GBW and SR depend only on the bias current of a transistor. FOM_S and $IFOM_S$ are the indications of the small-signal behavior of the amplifier, and FOM_L and $IFOM_L$ illustrate the large-signal behavior of the amplifier. Nonetheless, these four FOMs are actually inadequate to qualitatively evaluate a frequency compensation scheme, because the stability is also a critical criterion to impact the quality of a frequency compensation performance and should be taken into account for frequency compensation design.

IV. CONCLUSION

The operational transconductance amplifier is designed to drive a large capacitive loads. To operate the OTA under low-supply voltage bulk-biasing technique employed. A signal-current enhancers is employed in this paper. The cascade structure of six signal current enhancers is applied to a standard OTA to improve its GBW, SR, and voltage gain through the enhancements of the small-signal and transient output currents from the enhancers, The GBW and SR are improved by a factor of a $m(2K+1)^6$ and $m(K+1)^6$, respectively, the simulation results have fully verified performances scheme.

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