Design and Analysis of 8-T and 5-T based XOR and XNOR gates using Soft Computing Tools

Sowmya Bhat
Assistant Professor,
Department of Electronics & Communication Engineering
Shri Madhwa Vadiraja Institute of Technology and Management, Bantakal, Udupi, India

Sandesh Kumar
Assistant Professor,
Department of Electronics & Communication Engineering
Shri Madhwa Vadiraja Institute of Technology and Management, Bantakal, Udupi, India

Avinash N J
Assistant Professor,
Department of Electronics & Communication Engineering
Shri Madhwa Vadiraja Institute of Technology and Management, Bantakal, Udupi, India

Kusuma Prabhu
Assistant Professor,
Department of Electronics & Communication Engineering
Shri Madhwa Vadiraja Institute of Technology and Management Bantakal Udupi, India

Renita Pinto
Assistant Professor,
Department of Electronics & Communication Engineering
Shri Madhwa Vadiraja Institute of Technology and Management,
Bantakal, Udupi, India

***Abstract*— XOR and XNOR gates are the basic building block of arithmetic and logic circuits. In the modern era, VLSI technology demands the circuit design with least area consumption, least power consumption and high speed in operation. There are various CMOS logic structures available to design digital VLSI circuits, like, pass transistor logic, transmission gate logic, pseudo NMOS logic, CMOS logic, dynamic and domino CMOS logic, clocked CMOS logic, CVSL logic and so on. This paper presents the design of XOR and XNOR gates using pass transistor logic. Simulation results obtained in the mentor graphics tool are used to compare the number of transistor usage, area consumption, delay between 8-T and 5-T based XOR and XNOR gates and it proves that 5-T based design is the best in all the above-mentioned parameters.**

Keywords—Pass transistor logic; XOR and XNOR gates; area; delay

I. INTRODUCTION

Nowadays, the primary concern for any Very Large-Scale Integration (VLSI) system designers focuses mainly on System on Chip (SoC) design of VLSI circuits pertaining to minimum transistor count, thereby reducing the area consumption, power consumption, which is a crucial factor to be taken into consideration in case of any processor. XOR and XNOR gates are the fundamental components in designing of VLSI based circuits like adders, multipliers, comparators, multiplexers, demultiplexers, phase locked loop and so on.

Henceforth, a careful design and analysis is very much essential in designing these building blocks of VLSI circuits that is, designing XOR and XNOR gates. There are several Complementary Metal Oxide Semiconductor (CMOS) logic structures like pass transistor logic, transmission gate logic, dynamic CMOS logic, domino CMOS logic, clocked CMOS logic, cascade voltage switch logic (CVSL) available for designing digital VLSI circuits. Each type is having its own advantages and drawback. Since our main intention is to reduce the transistor count, in this paper we present a detailed design of XOR and XNOR gates using pass transistor logic by making use of 5 transistors and 8 transistors [1] thereby simulating and analyzing various performance parameters which needs to be taken into consideration for ease of design (simplicity) as well as better performance.

II. RELATED WORK

There are several techniques applicable to design XOR and XNOR gates which have its own advantages and drawbacks. Depending upon the designer and end user requirement, suitable CMOS logic structures. Pass transistor logic is a series combination of a set of transistors. Pass transistors can be categorized as PMOS pass transistor logic and NMOS pass transistor logic. PMOS pass transistor can pass good logic 1 whereas NMOS pass transistor can pass exact logic 0. Due to threshold voltage effect, PMOS and NMOS pass transistors are not capable of passing good logic 0 and logic 1 respectively. However, by connecting the substrate terminal of PMOS transistor to VDD and substrate terminal of NMOS to ground, this effect can be minimized to some extent. Due to minimal transistor usage in case of pass transistor, in this paper we have implemented the design of XOR and XNOR gates using this logic.

Pass transistor logic based XOR and XNOR gates and Complementary Metal Oxide Semiconductor inverter proved to dissipate less power, speed in operation and lower power delay product [2] when compared to design with a lower supply voltage [3].Usage of VDD and ground connection in the design of 6 transistor based XOR and XNOR gates using pass transistor has proved to have better driving capability and

full output voltage swing [4]. Advanced version of design in [4] was implemented in [5] using additional transistors to overcome the problem of logic degradation and proven to have better noise immunity and power delay product.

III. PROPOSED WORK

The Boolean expression used to design XOR and XNOR gate is given by the expression:

A XOR B = A'B+AB'

A XNOR B = A'B'+AB

The truth table explaining the above expression is as stated in the Table I below which states that XOR and XNOR logic operation is complementary to each other.

TABLE I. TRUTH TABLE FOR XORAND XNOR GATES

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

In this paper, design implementation of XOR-XNOR gates are accomplished using 8 transistors and 5 transistors. Table II states the working operation of XOR and XNOR gates using 8 transistors as shown in the Fig.1 representing schematic and Fig.2 representing the simulation circuit.

TABLE II. OPERATION TABLE FOR XORAND XNOR GATES DESIGN USING 8-T

A	B	MP1	MN2	MP3	MP5	MP4	MP2	MN 1	MN 3	XOR	XNOR
0	0	ON	OFF	ON	OFF	ON	ON	OFF	OFF	0	1
0	1	ON	OFF	OFF	ON	OFF	ON	OFF	ON	1	0
1	0	OFF	ON	ON	ON	OFF	OFF	ON	OFF	1	0
1	1	OFF	ON	OFF	OFF	ON	OFF	ON	ON	0	1

Design implementation follows the usage of CMOS inverter and pass transistor logic of both PMOS and NMOS type.

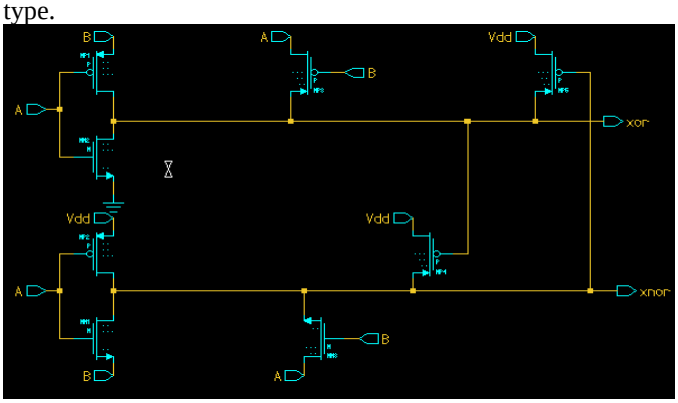

Fig. 1. 8-T Schematic Diagram for XOR-XNOR Gate Design

This type of design consumes large amount of space in terms of number of transistors usage because CMOS logic requires transistors equivalent to twice the number of inputs. Since PMOS and NMOS pass transistors are used problem is quite common regarding degradation of logic 0 and logic 1 states.

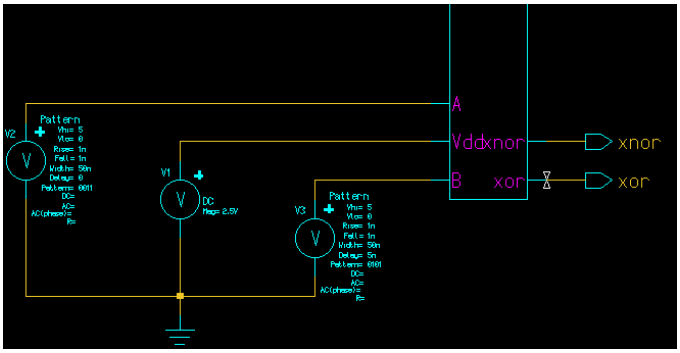

Fig. 2. 8-T Simulation Circuit for XOR-XNOR Gate Design

To overcome the problem of 8 transistors discussed above, XOR and XNOR gate design using 5 transistors was implemented wherein VDD and ground connection was considered for PMOS and NMOS pass transistor respectively to avoid the corresponding threshold voltage effect to certain extent as shown in Fig.3 representing the schematic diagram and Fig.4 representing the simulation circuit diagram for the design of XOR and XNOR gates.

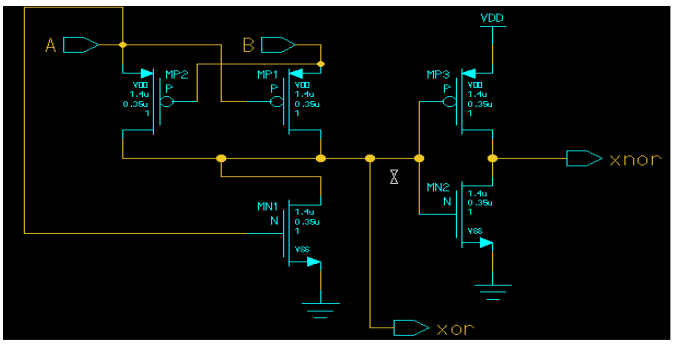

Fig. 3. 5-T Schematic Diagram for XOR-XNOR Gate Design

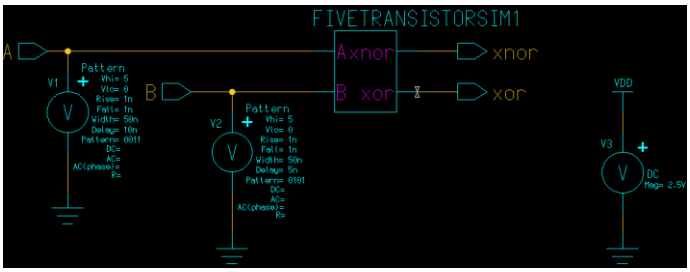

Fig. 4. 5-T Simulation Circuit for XOR-XNOR Gate Design

Table III explains the working operation of 5 transistor design.

TABLE III. OPERATION TABLE FOR XOR AND XNOR GATES DESIGN USING 5-T

A	B	MP2	MP1	MN1	MP3	MN2	XOR	XNOR
0	0	ON	ON	OFF	ON	OFF	0	1
0	1	OFF	ON	OFF	OFF	ON	1	0
1	0	ON	OFF	ON	OFF	ON	1	0
1	1	OFF	OFF	ON	ON	OFF	0	1

IV. RESULT ANALYSIS

Simulation results for transient analysis of design of XOR and XNOR gate has been obtained using 8 transistors and 5 transistors in tsmc018 technology using Mentor Graphics tool as shown in the below Fig.5 and Fig.6 respectively.

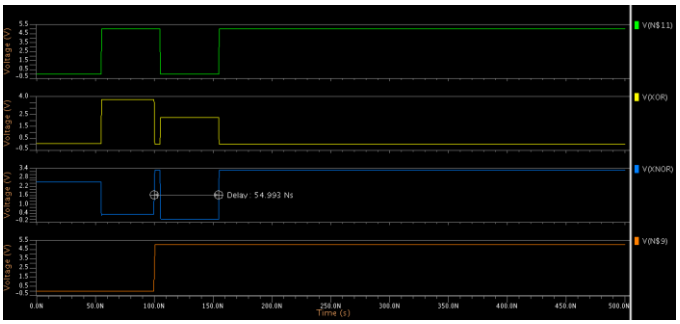

Fig.5 . 8-T Simulation Result for XOR-XNOR Gate Design

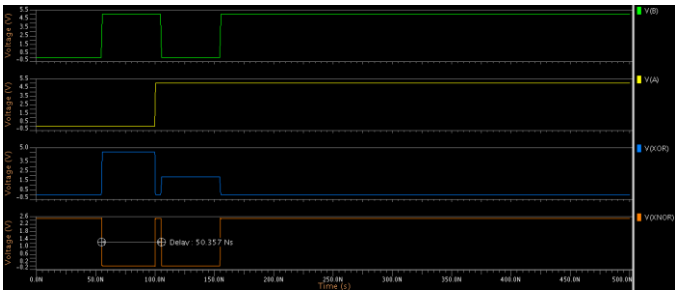

Fig.6 . 5-T Simulation Result for XOR-XNOR Gate Design

V. CONCLUSION

TABLE IV. COMPARISON TABLE FOR XOR AND XNOR GATES DESIGN USING 8-T AND 5-T

Parameters	**8-T**	**5-T**
Number of Transistors	8	5
Delay	54.993ns	50.357ns
Technology	tsmc018	tsmc018
Power Delay Product for XOR	16fJ	5fJ
Power Delay Product for XNOR	16.65fJ	4.5fJ
Area Consumption	3.92pm^2	2.45pm^2

The above Table IV represents the comparison between XOR and XNOR gates design using 8-T and 5-T.It is observed that area consumption in terms of number of transistors is more in second method when compared to first one. Delay is found to be 54.993ns and 50.357ns respectively. Hence operating speed will be higher for 5 transistor method when compared with 8 transistor implementation method. Hence 5 transistor method is found to be the best in terms of number of transistors, area consumption, delay and operating speed.

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