4H-SiC MOSFET H3TRB Long-Term Reliability Test

Tsz (Jim) Tsoi
Electrical and Computer Engineering Department,
Texas Tech University, Lubbock, TX, USA

James R Phillips
Electrical and Computer Engineering Department,
Texas Tech University, Lubbock, TX, USA

Stephen Bayne
Electrical and Computer Engineering Department,
Texas Tech University, Lubbock, TX, USA

Abstract— **The rising demand for long-term reliability for transistors in the integrated circuit causes the semiconductor industries to invest the long-term reliability technology in the extreme environment and static characteristics. A semiconductor device's passivation protects against external charges to interfere with the semiconductor material. The long-term reliability of semiconductor devices becomes critical in harsh environmental conditions with high-voltage applications. For many commercial 4H-SiC devices, the passivation layers contain Si3N4 or SiO2 over the edge termination area. The H3TRB (High Temperature, High humidity, and High Voltage Bias) test challenges a semiconductor device's long-term reliability in an extreme environmental chamber. The positive electric charges from the humidity and the extreme environmental condition create a chemical reaction over the passivation to cause a device's catastrophic failure. The paper analyzes the 4H-SiC devices tested in the H3TRB reliability test to evaluate the failure mechanism in the humidity environment.**

Keywords—Semiconductor Device; Wide-Bandgap; 4H-SiC; Reliability Test

I. INTRODUCTION

Wide-bandgap semiconductor materials become critical for the newly developing semiconductor devices in the electrical circuit, such as electronic and pulsed applications. The research materials such as 4H-SiC and GaN contain a couple of physical properties more advantageous than the Si material. In addition, most semiconductor devices accommodate Si material [1]. The figure below summarizes the fundamental property of semiconductor device application. The 4H-SiC and GaN materials have a higher bandgap, electric field, and melting point than the Si material. Also, the Si material has a higher thermal conductivity than the GaN material. The difference between the 4H-SiC and GaN, the GaN material has a higher electrical field and electron mobility. And the 4H-SiC material has a better melting point and thermal conductivity than GaN. So, the best semiconductor material currently in the market for power electronics applications is 4H-SiC due to the property of bandgap and thermal conductivity, which means that the heat can transfer faster in the material at high power applications. [2] The semiconductor devices for reliability would be 4H-SiC due to the high demand in power electronics applications.

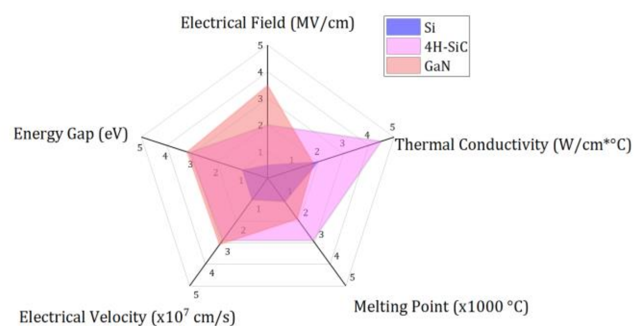

Fig. 1. Semicondcutor material comparsion [2]

This paper will discuss the semiconductor device: power MOSFET (Metal Oxide Semiconductor Field Effect Transistor). This device operates as an electrical switch, and the Vgs control the device's off-on state with the Vds larger value than the Vgs. The gate at the MOSFET contains a thin oxide layer, so the MOSFET only requires a minimal amount of current to drive the device. [3] The 4H-SiC MOSFET in this paper is rated for 1.2 kV and 20 A. Typically, a 4H-SiC MOSFET operates between 650 V to 1.7 kV [1] compared to Si only between 0 V to 200 V [4] with a larger device size due to the bandgap of the materials from figure 1. The contract structures displayed in Figures 2 and 3 below for a power MOSFET compared to the N-P-N MOSFET. The power MOSFET is a vertical structure that withstands a higher voltage than the horizontal N-P-N MOSFET and becomes more suitable for pulse power and power electronic applications.

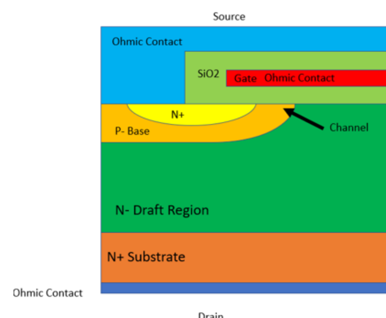

Fig. 2. Power D-MOSFET half-cell structure [1]

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 12 Issue 04, April-2023

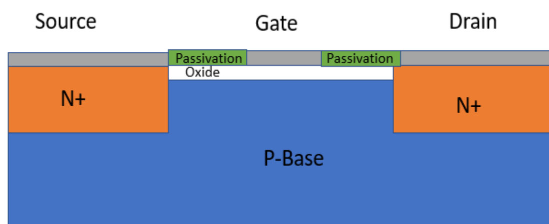

Fig. 3. Si N-P-N MOSFET structure. [3]

The tested power MOSFET in this paper contains the TO-247-3 package. This package is a standard package for the commercial transistor market. Also, this package allows designers to install a heat sink for heat management. The transistor's chip includes passivation, which contains SiO2 and Si3N4 over the top of the chip. [5] The internal package contains an encapsulation to protect the transistor die from external charge and containment. Figure 4 below shows the structure of a TO-247 series of transistor packages. The substance for the encapsulation includes a majority of the silica. The die-attach of the substance includes the Pb (Lead) and Sn (Tin). The bonding wire contains the Al (Aluminum). [6] The physical package and the passivation protect the transistor's chip from the extreme environment.

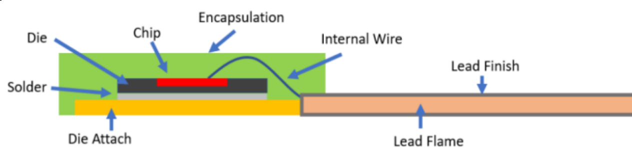

Fig. 4. TO-247 package layout [7]

The reliability test for extreme environment conditions used for the 4H-SiC MOSFET is H3TRB (High Humidity Temperature and High voltage Reversed Bias Test). This test challenges a semiconductor transistor's package's insulation ability and long-term reliability. So, the test result allows the engineer to evaluate the engineering application's transistor. The test is based on the JEDEC (Joint Electron Device Engineering Council) JESD22-A101; the devices were tested at 85 °C and 85% humidity for 1,000 hours testing period. [8] The JEDEC standard is a semiconductor transistor industrial standard for reliability. [9] The high temperature and high humidity create a chemical reaction environment for water diffusion into the package and passivation. The chamber temperature accelerates the water particles to diffuse from high-concentration to low-concentration areas. [8, 10 & 11] The environment condition evaluates the 4H-SiC power MOSFET for the device's reliability research purpose.

This paper provides the H3TRB test results for the 4H-SiC power MOSFETs for evaluation. The data allows engineers and students to understand 4H-SiC power MOSFET's performance in extreme environmental conditions. The data allows semiconductor device engineers to improve the passivation design against external influence and long-term reliability. The H3TRB test setup will be presented in the section below. A further discussion will analyze the failure mechanism, internal failure device structure, and the chemical reaction that causes a device's failure in the H3TRB test.

II. EXPERIENCE SETUP

The H3TRB test requires a test plan and document of a long-term period for the 4H-SiC power MOSFET. The components of the test include a PCB testbed, humidity chamber, and high-voltage power supply. The PCB testbed is based on the circuit schematic in figure 5. The board connects the gate and source of the devices. And the gate and source of the MOSFETs connect to the GND. So, the devices are hold-off voltage throughout the test period. The chamber and power supply are shown in figure 6. The humidity chamber model is TPS T2RC-A-F4T. The chamber is rated for -68 °C to 180 °C, and the humidity level is rated for 20% to 95%. The high-voltage power supply is Spellman SL60. The supply is rated from 0 to 60 kV with a current of 0.5 mA. The high-voltage power supply is located outside the chamber. The PCB board can contain a total of fifteen devices during the test. However, this paper only presents eight devices shown in figure 5. Every component operates the H3TRB test to challenge the 4H-SiC power MOSFET long-term reliability.

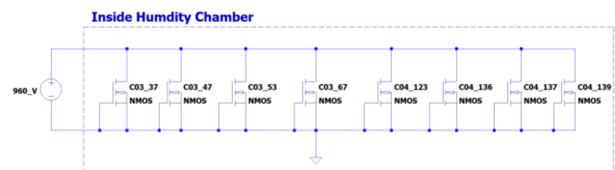

Fig. 5. H3TRB test circuit schematic

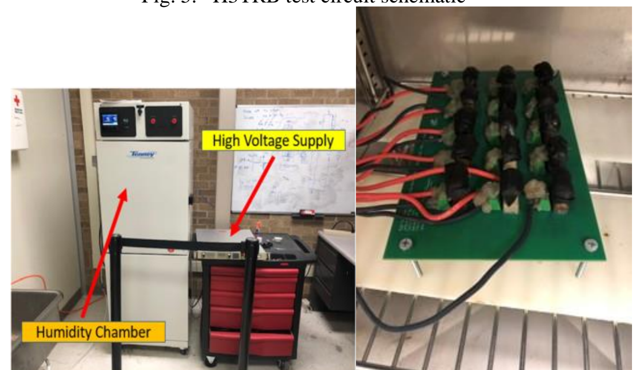

Fig. 6. H3TRB test setup (Righ side: chamber and high voltage supply; Left side: H3TRB board PCB)

The test plan of the H3TRB test stages the power MOSFETs to compare the initial static characteristics before and after the reliability test. The comparison data presents a device's reliability performance and evaluate a device's current characteristics. First, all the devices were placed at Agilent Technologies B1505A Power Analyzer for static characteristics such as forward I-V and reversed breakdown. Next, all the devices are placed at the H3TRB testbed in figure 6. Third, the chamber is set at 85 °C with 85 % humidity. The power supply is set at 850 V. This voltage is 80% of the device's rating according to JEDEC standards. Fourth, the devices would wait a thousand hours or until a failure. A failure device defines a device's short circuit that's shown from the power supply. Ultimately, the devices are placed in the power analyzer for final static characterization. All the failure devices would send microscope images for further evaluation. The documents of

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 12 Issue 04, April-2023

devices and microscope images provide evaluations of the 4H-SiC MOSFETs in extreme conditions.

III. TEST RESULT AND FAILURE MECHANISM OUTCOME

This section discusses the H3TRB test result and the plausible reason for the device's failure. The first part documents each tested 4H-SiC power MOSFET from the reliability test, and the second part documents each failure device top view structure to explain the failure location. The section also discusses the electrochemistry over the passivation layers and compares some previous studies for the possible mechanism to cause the short circuit on the device. The presented data informs the tested 4H-SiC power MOSFETs' evaluation from the reliability test.

TABLE I. TESTED DEVICE DOCUMENT

Device #	H3TRB Test Result
	Pass/Failure
1	Failure
2	Pass
3	Pass
4	Failure
5	Pass
6	Pass
7	Pass
8	Pass

Table 1 presents all 4H-SiC power MOSFET's tested results over the H3TRB test. The table defines a "Pass" as a device that survives 1,000 hours of H3TRB testing, and a "Failure" defined as degraded and catastrophic failure devices during and after the H3TRB test. The table shows only two catastrophic failure devices during extreme conditions; the other six devices define a" Pass" in the H3TRB test. Both devices do not hold off voltage breakdown during static characterization measurement. The rest of the "Pass" device can still hold off 650 V in characterization measurement. The figures below show the failure devices' structure and location of degraded passivation. Figure 7 shows the first degraded device. The short circuit occurs at the gate location and the edge termination. On the second device, the picture covers the second degraded transistor in figure 8. The short circuit occurs at the top left over the edge termination. Both devices appear to have short circuits around the edge termination. However, the first device has a "short circuit" around the gate, and the other only has the top edge. So, the second device can still achieve a forward I-V curve and the threshold voltage measurement. The degraded transistor shows the vulnerability of the passivation and package in H3TRB environmental conditions.

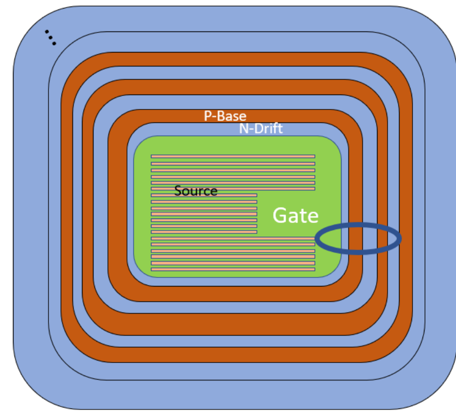

Fig. 7. First failure device structure

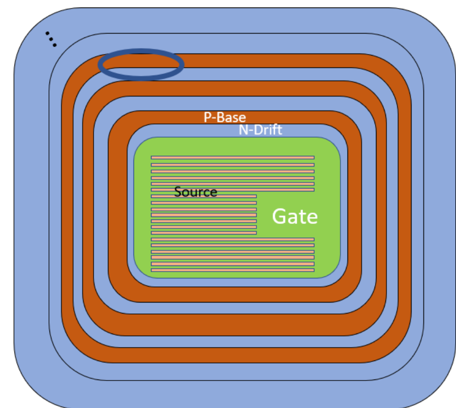

Fig. 8. Second failure device structure

The water particle chemical reaction influences the two devices' degradation in the H3TRB test. It creates a diffusion of charge carrier over the passivation to cause the short circuit. The water diffuses through the package and the passivation. And the water begins hydrolysis as the elevated temperature and high field in the passivation layers. Water hydrolysis is a chemical reaction of water from liquid to gas form. As hydrogen and hydroxide ions separate, impurities such as Pb (lead) mix with water particles, creating a water tree from the anode and the cathode side. [12] The water tree is a degradation over the insulation due to moisture interference with water particle reaction with different chemical defects. [13] Once the water tree from both sides grows at a certain distance, the high field would cause a short and new current path at the passivation, increasing the leakage current in the breakdown cure. The leakage current equals the space charge generation and diffusion current over the P+ and N+ regions. Since the insulation has a current path from the water tree, that creates an added current from the passivation layer to the device's leakage or breakdown curve. [12 & 14] The influence of moisture proves the critical factor for the passivation layer in a 4H-SiC power MOSFET.

IV. CONCLUSION

The H3TRB test results over the 4H-SiC power MOSFET prove the capability and resilience of the package and passivation in the extreme humidity environment during high field application. The microscope image of the tested transistor shows the damage over the edge termination of the die. The water particles influence the passivation of the edge termination

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

and react with the lead (Pb), creating the water tree at the anode and cathode side over the insulated passivation to cause a different current path and increase the leakage current. The damaged power MSOFET provides evidence for researchers and engineers to awaken the humidity condition in power electronic and pulsed power application designed circuit.

ACKNOWLEDGMENT

I want to acknowledge Dr. Stephen B. Bayne for sponsoring this project.

REFERENCES

[1] B. J. Baliga, “Fundamentals of Power Semiconductor Devices”. Cham: Springer International Publishing, 2019.

[2] Bieniek, Tomasz & Janczyk, Grzegorz & Sitnik, Adam & Messina, Angelo. (2019). The "first and euRopEAn siC eigTh Inches pilOt line" - REACTION project as a Driver for key European SiC Technologies focused on Power Electronics Development.

[3] Robert H. Crawford, “MOSFET in Circuit Design: Metal-Oxide Semiconductor Field-Effect Transistors for Discrete and Integrated-Circuit Technology”. Texas Instrument Electronics Series, McGraw-Hill Book Company.

[4] N. Mohan, T. M. Undeland, and W. P. Robbins, “Power Electronics: Converters, Applications, and Design”. Hoboken, NJ: John Wiley & Sons, 2003.

[5] B. M. Green and H. S. Henry, “Transistor and Method with Dual Layer Passivation,” U.S. Patient. 05-Jun-2012.

[6] Central Semiconductor Corp., “Material Composition Specification: TO-247 Case”

[7] C. A. Harper and E. M. Petrie, Plastics materials and processes: a concise encyclopedia. Hoboken, NJ: Wiley-Interscience, 2003.

[8] J. Jormanainen et al., "High Humidity, High Temperature and High Voltage Reverse Bias - A Relevant Test for Industrial Applications," PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2018, pp. 1-7.

[9] JEDEC, “Why JEDEC Standards Matter” Website: https://www.jedec.org/standards-documents/about-jedec-standards

[10] J. W. Osenbach, “Water-Induced Corrosion of Materials Used for Semiconductor Passivation”. AT&T Bell Laboratories, Solid State Technology Center, Breinigsville, Pennsylvania 18031

[11] Valérie Guillard , Claire Bourlieu , Nathalie Gontard, “ Food Structure and Moisture Transfer: A Modeling Approach”. Publisher: Springer Link.

[12] J. Leppanen, G. Ross, V. Vuorinen, J. Ingman, J. Jormanainen, M. Paulasto-Krockel, “A humidity-induced novel failure mechanism in power semiconductor diodes”, Microelectronics Reliability, Volume 123, 2021, 114207, ISSN 0026-2714, https://doi.org/10.1016/j.microrel.2021.114207.

[13] J. L. Chen and J. C. Filippini, "The morphology and behavior of the water tree," in IEEE Transactions on Electrical Insulation, vol. 28, no. 2, pp. 271-286, April 1993, doi: 10.1109/14.212252.

[14] B. N. Pushpakaran, S. B. Bayne, “Modeling and Electrothermal Simulation of SiC Power Devices Using Silvaco ATLAS” in World Scientific

(This work is licensed under a Creative Commons Attribution 4.0 International License.)