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30 GHz Front–End in 40 nm CMOS Technology for 5G Phased Array Systems

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***Abstract*—This paper presents an RF front-end with enhanced performance, operating at 30 GHz for Phased Array systems in 40nm CMOS. The proposed transmitter-receiver front-end consist of a low-loss (0.65dB) SPDT Switch, a high gain 31.3dB Low Noise Amplifier, and a Power Amplifier with output power of 19.45 dBm. The front end includes variable gain amplifiers (VGA) and phase shifters (PS) exhibiting programmable gain of 13dB and phase control of 360º in steps of 22.5º. The overall front-end fully satisfies 5G requirements.**

***Keywords*—RFIC, LNA, PA, Phase Shifter, Phased Array, 5G, VGA, SPDT switch, front-end**

I. INTRODUCTION

Due to the growing need for 5G high speed networks, the development and implementation of high-performance electronic systems and transceivers is becoming increasingly important. In order to satisfy such speeds, multiple-input multiple-output (MIMO) systems are required. These systems use phased arrays [1] and beamforming systems to achieve the demands of the 5G network.

The increased cut-off frequency (f_T) of CMOS technology and the capability to integrate the entire system in a chip, accelerated the demand of radio frequency (RF) front-ends in millimeter-wave (mm-wave) frequencies. The demanding specifications of 5G systems at frequencies such as 30 GHz render the design of the front-end extremely challenging, especially for the Low Noise Amplifier (LNA) and the Power Amplifier (PA). On the receiver chain (RX) the Low Noise Amplifiers should be able to present high gain, low noise figure (NF) and input/output matching throw the entire 5G band. On the transmitter (TX) side the Power Amplifier has to present adequate gain combined with high linearity and high output compression point.

The majority of 5G front-ends in mm-wave systems incorporate a variable gain amplifier (VGA), a phase shifter (PS) and a power amplifier (PA) in the TX side [2]. The RX side consists of the Low noise amplifier (LNA) followed by a PS and a VGA. The proposed RF front-end is presented in Fig. 1. Recent standards for 5G demand programmability 360º in phase, so the PS controls the transmission phase angle of their input signal. In addition to phase control, gain control needs to be performed.

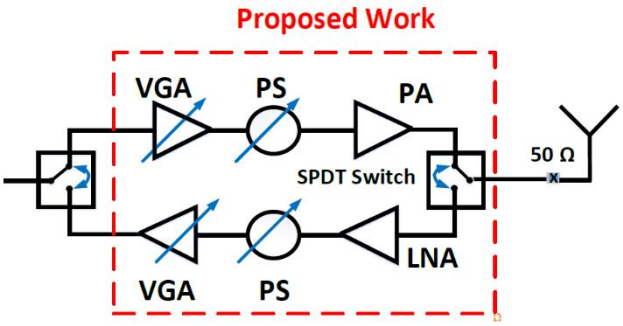

Fig. 1. Block diagram of the proposed RF front-end

Thus, the use of VGA is a necessity not only to give the ability of controllable gain, but also to mitigate the losses of the phase shifters. Finally, a pair of switches is necessary to connect the front-end to the antenna and the back-end section of the transceiver.

The proposed RF front-end is suitable for phased array 5G systems as it exhibits approximately 20 dBm of Psat at the transmitter output, a noise figure of 6 dB at the receiver. Furthermore, it includes VGAs and phase shifters providing 13 dB gain variability and full 360^o phase variation respectively, Due to the above, the overall front-end exhibits enhanced performance comparable with state-of-the-art radios in the literature, rendering tit suitable for beam-stirring systems for 5G protocols [3].

II. CIRCUIT DESCRIPTION

A. Switch

In half-duplex 5G front-ends the first passive component after the antenna is the switch. Transmitter/Receiver (T/R) switch provides an effective way to select which chain between the RX or TX will be active and additionally separates and isolates the two chains. As a result, switch enables sharing of a single antenna between the T/R front-end reducing chip size and cost. The most common switch type used in such systems is the single poll double throw (SPDT) switch [4]. A series-shunt SPDT switch is used and in the proposed RF front-end. The switch should present high isolation. Isolation, which is determined by the signal's amplitude coupled over a cut-off transistor device. When the devices are off, their junction and parasitic capacitances have a significant impact on it. Moreover, should present low insertion losses, for that reason devices with low Ron are used in the SPDT switch to minimize the power losses on the

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switch. Finally, of paramount importance is and the linearity of the switch and especially on the TX devices. The SPDT switch is significant to has adequate linearity to handle the power of the transmitted signal of the PA [ref]. In the proposed switch the isolation is 25.3 dB the insertion losses are less than 0.65 dB both on the RX and The TX side and is obtained high linearity with P1dB: 30dBm.

B. LNA

The proposed LNA topology consists of three stages as is depicted in Fig. 2. All stages are in cascode configuration. The cacsode configuration is chosen in order to utilize the advantages which offers. Cascode amplifiers consist of a Common Source (CS) and a Common Gate (CG). Cascode, compared to the CS amplifiers exhibit higher gain due to the mitigation of the Miller effect with the use of CG transistor. Additionally, cascode configuration presents better input/output isolation. As a result, the reverse isolation and the stability of the amplifier are significantly improved. The design objective of the first cascode stage (M1 and M2 transistors) is to achieve the lowest possible noise figure. This is because the first stage of an amplifier is the one contributing the most in noise figure of the overall RX chain [5]. Thus, the design of the devices is accomplished to achieve the minimum NF. The bias voltage (VG1) of M1 transistor is selected at 520 mV for the optimum Noise Figure profile. Furthermore, input matching with the 50 Ohm antenna load is accomplished at the first stage of the Amplifier. The input matching network consists of an inductor (L1) and a capacitor (C1). To achieve wide band input matching covering the entire 5G band, a degeneration inductor (L2) is used at the source of M1 transistor. The price paid for the inductive degeneration is gain reduction. The input matching (S_{11}) remains better than -10 dB from 23.2 GHz to 32.5 GHz. The gate voltage of M2 (VG2) is chosen to be equal to VDD (at 1V). The power consumption of the first stage is 12 mW and provides a gain of 7.9 dB.

The second and third cascode amplifier-stages are designed in order to provide gain to satisfy the 5G protocol specifications. The first stage is connected to the second through a transmission line (TL1) as well as the second with the third stage (TL2). In second and third stages there is no need for low NF and input matching with the antenna, but they should offer sufficient gain instead. The length of the transmission lines TL1 and TL2 is selected in that way to accomplice inter-stage matching between the amplifiers due to the added inductance. Capacitors C2 and C3 apart from assisting in inter-stage matching act as DC-blocks as well. The VG3 and the VG5 are selected at 450 mV and 470mV respectively and the VG4 and VG6 at VDD voltage. The second stage provide a gain of 11.3 dB and the third a gain of 12.1 dB with the entire LNA chain providing 31.3 dB of gain and consuming 26.4 mW of power. The Lint inductors in the design present the added inductance between cascode transistors due to the metal routing. The output matching is better than -10 dB at 30 GHz. The input and the output matching are illustrated in Fig.3.The gain (S_{21}) of the LNA (illustrated in Fig. 4.) remains above 21 dB presenting a 3-dB bandwidth from 23 GHz to 29.5 GHz with gain peak at 31.3 dB. The minimum Noise figure of the 3-stage amplifier as it is depicted in Fig. 5, is 4.37 dB. Finally, the Stability Factor (K) is calculated in order to evaluate if the amplifier is unconditionally stable (K>1). Simulations gave a minimum value for K equal to 22.

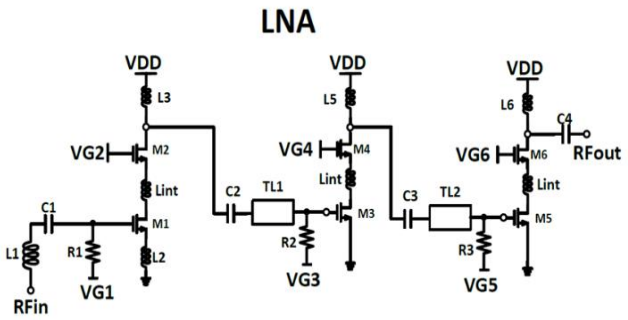

Fig. 2. Three-stage LNA schematic

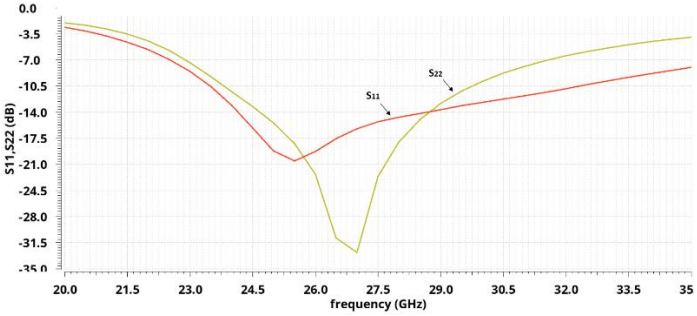

Fig. 3. Input/Output Matching of the LNA (S_{11}/S_{22})

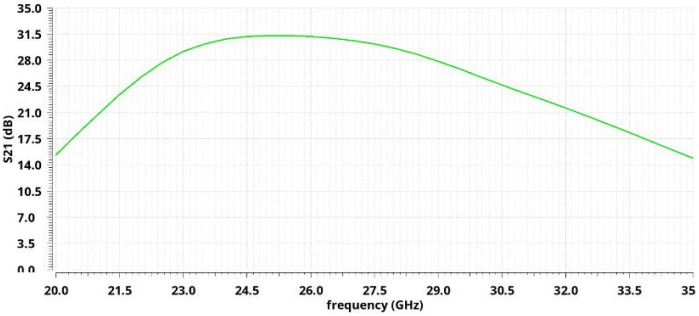

Fig. 4. Three-stage Gain (S_{21}) of the LNA

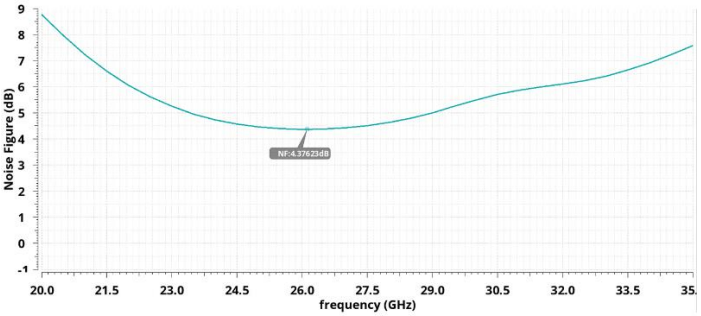

Fig. 5. Noise Figure of the LNA

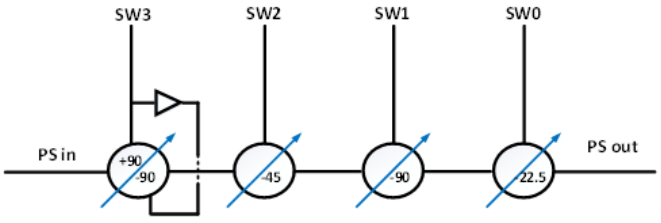

Fig. 5. Proposed Phase Shifter chain

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C. Phase shifter

The Phase shifter (PS) uses a switching type passive topology (STPS) to cover a full 360-degrees of phase shift. It contains 4 individual phase shift blocks, Fig. 6, that are connected in series. The placement of each block within the PS chain, is chosen to make input and output matching easier at 50 Ohm. There are 3 switching LC networks that provide- 22.5^{o}, -45^{o} and -90^{o}degrees angles. Each of these three individual blocks consists of a series and a parallel inductor to the RF path. In parallel of both inductors, switches are placed to switch on/off the inductance. The switches act like capacitors at the off state at mm-wave frequencies, providing the specific angle at the ON state. At the OFF state, the network just passes the RF signal without any phase alteration. For the 180 degrees, a plus/ minus 90 degrees LC network is used. Two LC pi-networks, a low-pass and a high- pass, are placed in parallel, and their operation is determined by switches. In other phase shifting works [6] the 180^{o} is produced by placing two 90^{o} blocks in series, which requires a lot of area and is worse in phase error. The dimensions of the switches have been chosen to minimize losses while keeping the isolation high enough. Finally, the PS uses the minimum number of inductors (nine) to achieve the 360-phase angle in a. The quality factor (Q) of the series inductors must be kept high while the parallel to the RF path inductors, which need to be of higher inductance, present a lower Q. The phase step of the PS is 22.5 degrees and is a standard for a 4-element architecture [7].

In Figures 6, 7 the phase angle and the insertion loss of all the possible combinations of the PS is shown. The loss reaches a max of 13 dB at 24 GHz. The PS delivers 360-degrees at a bandwidth of 8 GHz from 24-32 GHz. It is matched both at the input and output and the return losses are better than 10 dB across the band.

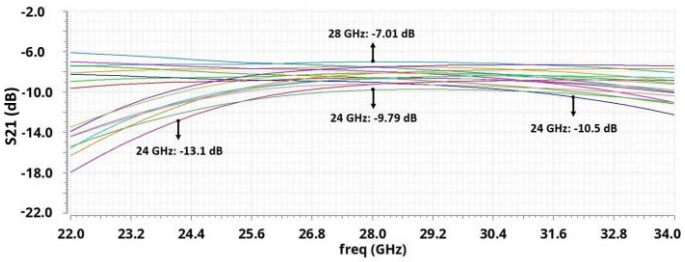

Fig. 6. Phase shifter loss across frequency

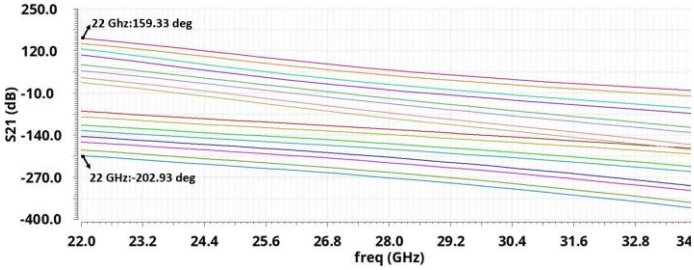

Fig. 7. Phase shift for every combination across frequency

D. Power Amplifier

The Power amplifier contains two differential stages, the driver, and the output stage (OS) [8]. The output stage is a two-stacked topology that uses capacitor neutralization technique (CNT) with intermediate inductance matching between the common-source and the common gate devices of the stacked architecture. The CNT provides better isolation, maximum gain and stability but lacks in bandwidth. The proposed design manages to overcome this drawback by tuning the interstage matching network between the driver and the OS. Moreover, the stacked configuration keeps the operation under safe regions while the supply voltage is set to 2 V. Before the OS a driver, following the same topology as the final PA, is placed to boost the gain and also to extend the bandwidth of the PA. The CNT is used also in this stage. Furthermore, in order to provide an easier input matching a degeneration inductor is also added at the source of the CS devices. The matching network (MN) at the output is designed based on load pull simulations for higher linearity while the interstage MN extends the achievable bandwidth. Finally, the input MN does not affect the output performance and is designed to match the input to 50 Ohm across the entire band. One additional critical element to the proposed PA is a dynamic bias at the gate of the CS of the output stage. This enhances linearity and back- off power added efficiency (PAE) with an increase in dissipation near compression point.

In Fig.8, S_{21} along with S_{11} is presented. Apart from the small signal analysis in Fig.9 the power gain of the PA along with the O1dB for the three main frequencies are illustrated. The output compression point is at 18 dBm for typical 80 C conditions and 28 GHz while it falls to 17 dBm at 32 GHz. Furthermore, Psat for 24, 28, 32 GHz is at 19.45 dBm, 19 dBm and 18.44 dBm respectively. The total consumption at max output power is 130 mW.

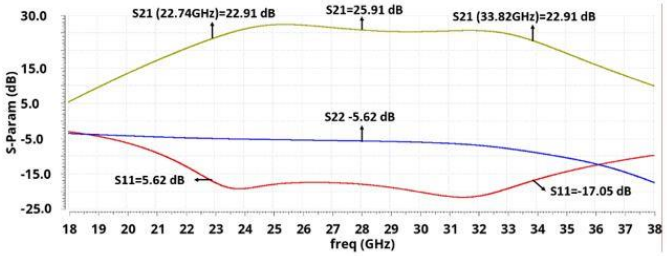

Fig. 8. Small signal analysis of PA

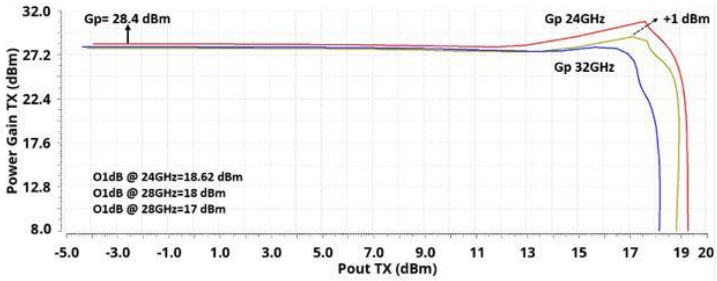

Fig. 9. Power Gain of PA

E. VGA

The VGA consists of 3 single-ended cascode stages. The main goal of the VGA is to eliminate the losses produced by the PS at every possible phase combination. The input of the VGA is connected to the PS and is well matched at 50 Ohm. Furthermore, its output is connected to the input of the PA and is also matched. The output matching contains a

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single- to -differential balun to feed the differential input of the PA while a 4 bit-capacitor bank is also placed for tuning purposes. The MNs between the 2nd and the 3rd stage improve the gain-bandwidth product and also contain cap. banks for tuning. Moreover, the supply of the VGA is at 1.1V to keep dissipation low. Current steering (CS) is the main technique used in the VGA. This technique is implemented at the first stage and contains an array of digitally controlled devices that enable the gain programmability of the VGA. In this CS topology, fifteen NMOS devices are used. Their source is connected to the intermediate node of the cascode topology of the first stage, while their drains are connected to the supply. When all devices are OFF they act as a capacitor. In this case the first stage provides the next with the maximum gain. When all are ON then the gain decreases and reaches minimum value. The devices are digitally controlled by a thermos logic and turn off one after the other providing with a good resolution and the needed back -off. The size of the CS cells is not the same. To keep the same gain step in the entire dynamic range, the cells must be larger as more and more are turned ON.

This specific VGA can provide 13 dB of gain at maximum operation with 7 dB total back off and a gain step of 0.5 dB. There are numerous alternatives regarding the gain programmability mechanism [9],[10]. However, the digitally controlled current steering cells used in this work provide easier controllability with a small gain step and high gain range. In Fig. 10 the small signal analysis of the VGA versus the frequency is shown. Finally, in Fig. 11 the gain at 28 GHz while changing the CS control word is also presented. The VGA covers adequately the losses of the PS and can be placed right after it. The total consumption at highest gain is 27.33mW.

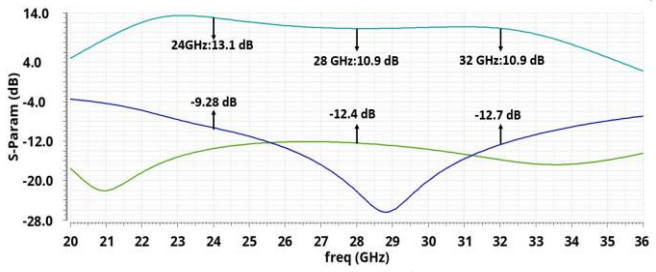

Fig. 10. S-parameters of VGA

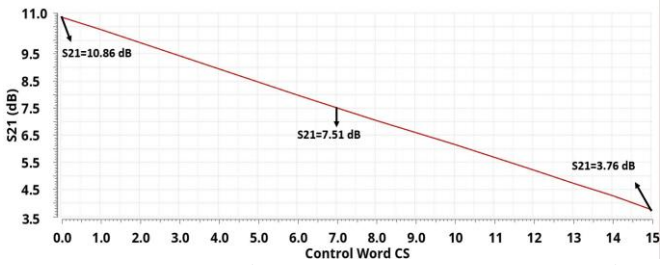

Fig. 11. Dynamic range of VGA at 28 GHz across all combination of CS

III. CONCLUSION

The RF front-end consists of high-performance passive and active components to fulfill the 5G demanding specification. The switch after the antenna exhibits low losses and high isolation between the TX and the RX. The LNA consist of three stages offering high gain of 31.dB. The Phase shifter follows a switched type topology achieving 360 degrees of total phase shift. The loss is below 13 dB with a phase step of 22.5 degrees. Furthermore, the Power amplifier uses a two-stage differential architecture with adaptive bias. It reaches a saturated output power of 19.45 dBm at 24 GHz and has a bandwidth of 8 GHz around 28 GHz. The dissipation of the PA is at 130 mW from a supply of 2 V.The VGA consists of a 3-stage single ended topology and manages to cover the losses of the PS at a maximum gain of 13 dB. The gain step is 0.5 dB and exhibits a gain range of 7 dB while consuming 27.33 mW. To conclude, a high-performance state of the art RF transceiver is presented to satisfy the specifications of 5G protocols with gain and phase programmability.

IV. ACKNOWLEDGMENT

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