

2. 4Ghz High Gain and Low Noise CMOS LNA

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Abstract—This paper presents the design of narrow band single stage Low Noise Amplifier (LNA) which is optimized for working in the 2.4 GHz frequency band range. The proposed LNA has been designed and simulated in RF-TSMC 0.18μm CMOS technology by Advanced Designed System (ADS). The designed LNA uses 1.8V supply voltage and it exhibits a gain of 24.253 dB, noise figure of 0.834 dB, input reflection coefficient (S11) of -12.89 dB, reverse gain (S12) of -30.27

Keywords—Advanced Design Simulation (ADS) Software, Low Noise Amplifier (LNA), Complementary MOSFET (CMOS)

I. INTRODUCTION

Due to the tremendous growth is wireless communication technology, the demand for highly integrated radio frequency circuits having low noise, high gain and low power dissipation is increasing.

Wireless systems comprise of a front-end and a back-end section. The front-end section processes analog signals in the high radio frequency (RF) range while the back-end section processes analog and digital signals in the baseband low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications. It lies typically from 100 KHz to 100 GHz. However in general, frequencies below 1 GHz are considered baseband frequencies while those greater are described as RF. The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver. Such an amplifier is referred to as a Low Noise Amplifier and forms an essential component of any RF integrated circuit receiver [1]. Low noise amplifier is the important and first block of RF receivers [2]. The signal received by the antenna is very small. In order to achieve good linearity, high gain and low power consumption, it is important to amplify the signal as much as possible without the addition of noise [3][4]. The most optimum tradeoff between various parameters has to be achieved for designing of LNA. Also, the size of communication devices and power consumption should be as minimum as possible, which is possible nowadays because of advancements in integrated circuit (IC) technology [5].

Several fundamental low noise amplifier topologies for single ended narrow band design are available, such as resistive termination common source, common gate, shunt series feedback common source, inductive degeneration common source, cascode inductor source degeneration [6].

The design is based on a inductive degeneration common source configuration This paper describes the operation and the simulation of s-parameters, gain and minimum noise figure using 0.18μm CMOS technology.

II. DEVICE SPECIFICATIONS

A. DC Biasing

Selection of transistor is essential in the first stage A CMOS 180 nm technology transistor with TSMC 0.18 micron CMOS logic process technology scale is utilized for realizing front-end designs . This device is biased to operate at $V_{ds} = 1.8$ V, $I_{ds} = 0.03A$. The value of gate-source voltage (V_{gs}) is obtained from I_D - V_{DS} characteristic curve, in quiescent point of transistor [7], which is shown in figure 1

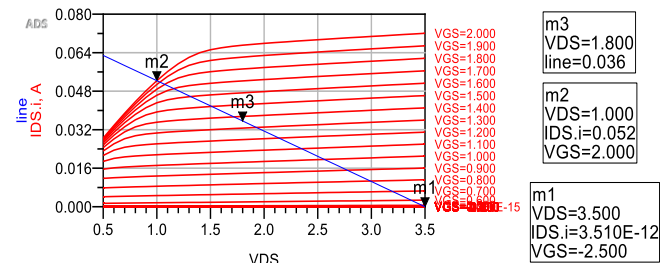


Figure 1- ID-VDS Characteristic curve

The DC biasing circuit that is employed for this simulation is shown in figure 2.

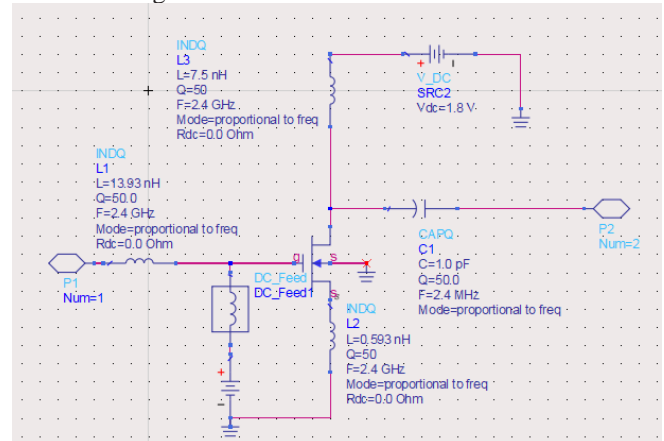


Figure 2- DC Bias Network

B. Stability

The Stability is the most important thing which needs to be considered when designing an amplifier. If stability is not designed properly, the amplifier would get self-excited and it cannot work rightly. Stability can be determined from the S parameters, the matching networks, and the terminations. To improve the stability a negative feedback is an effective technique is used. The source ground is connected with an inductance to form a negative feedback to improve the stability. It can be shown that the amplifier will be unconditionally stable if the following necessary and sufficient conditions are met [8].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11} \times S_{21}|^2} > 1 \quad (1)$$

$$\Delta = |(S_{11} \times S_{22}) - (S_{12} \times S_{21})| < 1 \quad (2)$$

C. Matching Network

In order to maximize power transfer from source to load, matching impedances is required. The input and output matching networks is designed using ADS smith chart utility. The open stub matching is used to design input and output matching networks.

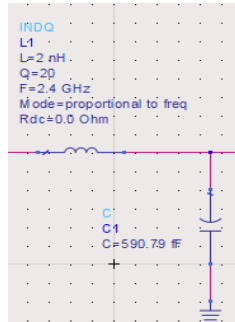


Figure 3. Input impedance matching

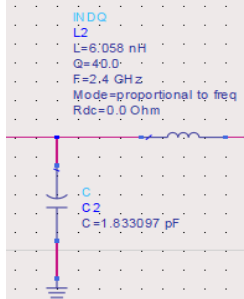


Figure 4. Input impedance matching

III. CIRCUIT DESIGN

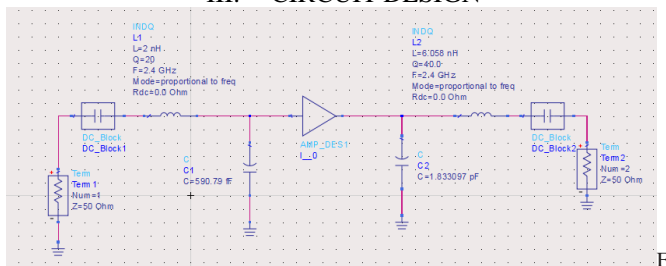


Figure 5. Schematic of proposed circuit in ADS

In the proposed LNA architecture employs inductive source degeneration to generate a real term in the input impedance. Tuning of the amplifier input becomes necessary, making this a narrow-band approach. The inductive source degeneration is the most prevalent method used for CMOS amplifiers. At the series resonance of the input circuit, the impedance is purely real and proportional to L_s . By choosing appropriately, this real term can be made equal to 50Ω . The gate inductance is used to set the resonance frequency once is chosen to satisfy the criterion of a 50Ω input impedance. L_1 and C_1 provides proper input matching and L_2 and C_2 provides output matching. Thus, the

proposed circuit provides high gain and low noise figure by maintaining good linearity.

IV. SIMULATIONS AND RESULTS

Simulations of the proposed LNA for 0.18 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S_{21}) of 24.253 dB as shown in figure 8. The input reflection coefficient (S_{11}) is -12.890 dB as shown in figure 6 and the output reflection coefficient (S_{22}) is -19.620 dB as shown in figure 9. The circuit operation requires 1.8 V power supply. The value of reverse isolation (S_{12}) as shown in figure 7 is -30.270 dB and a minimum noise figure of 0.834 dB is obtained as shown in figure 10. The simulated amplifier's characteristics summary is presented in Table I. From Table I, compared with other LNA's, the performance of our proposed CMOS LNA is much better as it has the best reported value of NF at 2.4GHz.

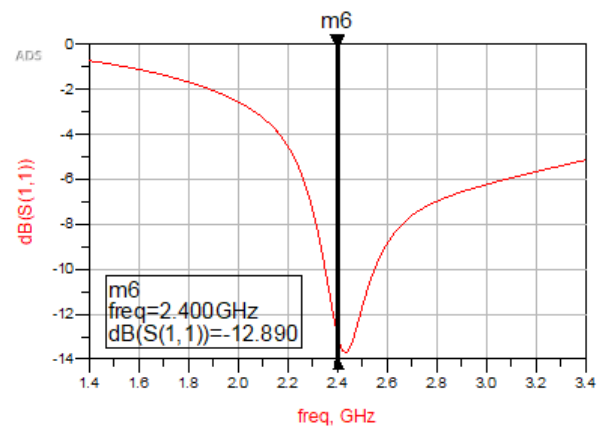


Figure 6- Input Reflection Coefficient (S11)

S_{11} (input reflection coefficient) also known as input return loss. It represents the measure of matching of the input impedance to the reference impedance. For 2.4 GHz, as shown in figure 6, the value of S_{11} is -12.890 dB.

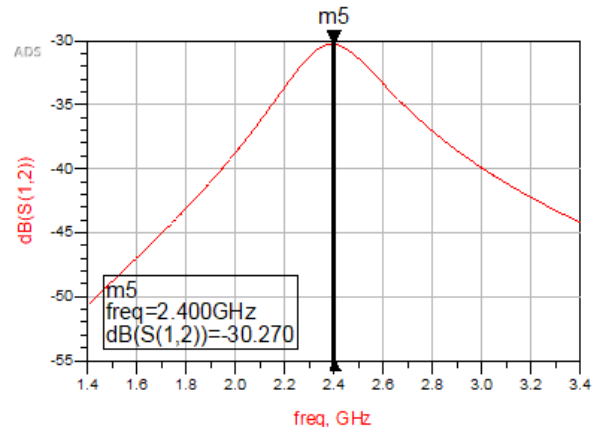


Figure 7- Reverse Gain/ Reverse Isolation (S12)

S_{12} (reverse transmission coefficient) also known as reverse isolation, it measures how much the input signal is reflected back. For 2.4 GHz, as shown in figure 7, the value of S_{12} is -30.270 dB. Hence, a high isolation is present between input and output.

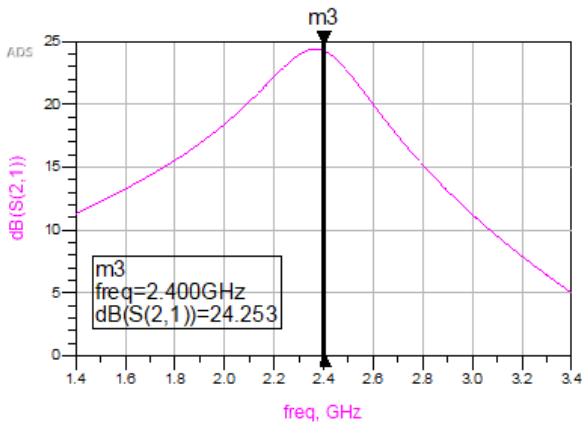


Figure 8- Forward Gain (S21)

S21 (forward transmission coefficient) also known as forward gain, it measures how well the signal goes from input to output. For 2.4 GHz, as shown in figure 8, the value of S21 is 24.253 dB. Therefore, the value of output voltage obtained is good even for a small value of input voltage

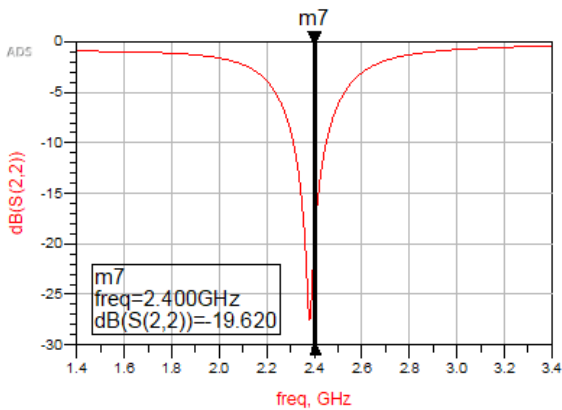


Figure 9- Output Reflection Coefficient (S22)

S22 (output reflection coefficient) also known as output return loss, it represents the measure of matching of the output impedance to load impedance. For 2.4 GHz, as shown in figure 9, the value of S22 is -19.620 dB indicating that a considerable matching of the output impedance to 50 Ω is obtained

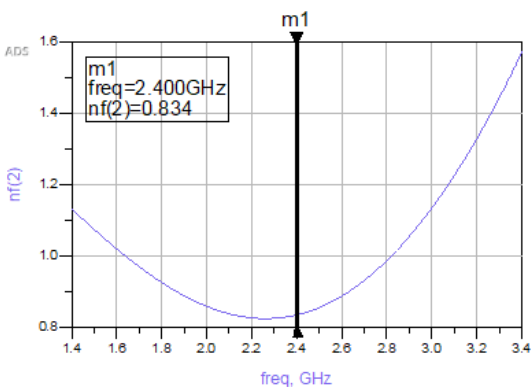


Figure 10- Noise Figure (NF)

The noise performance of device at high frequency is indicated by noise figure. The minimum noise figure of 0.834

dB has been obtained at 2.4 GHz, as shown in figure 10. This value indicates that the noise performance of the circuit is very high as the value of noise figure of the circuit is very low.

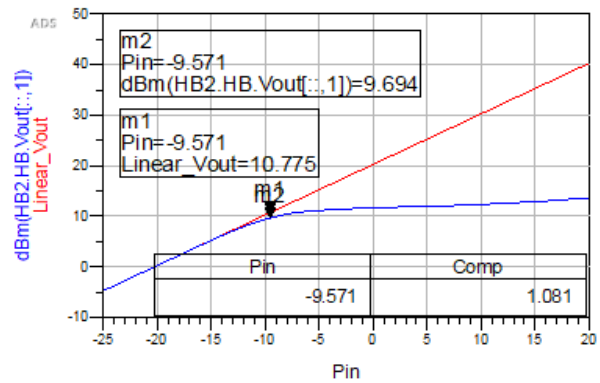


Figure 11- IIP3

LNA along with amplification of signal and good noise performance, should be linear even when the signal is strong. Hence, during designing of LNA, linearity is an important consideration. The third intercept point is illustrated in figure 11 that was achieved at -9.571 dBm.

TABLE I. COMPARISON OF DIFFERENT CMOS LNAs

	[9]	[10]	[11]	[12]	[13]	This Work
Frequency (GHz)	2.4GHz	2.4GHz	2.4GHz	2.4GHz	2.4GHz	2.4GHz
Technology (µm)	0.18µm	0.13µm	0.18µm	0.13 µm	0.13 µm	0.18 µm
Supply (V)	1.8V	1.2V	1.8V	1.2V	0.8V	1.8V
Gain (dB)	15.9dB	15.417dB	14.5dB	20dB	15dB	24.25dB
Noise Figure (dB)	1.8 dB	1.182dB	2.8dB	4 dB	3.6dB	0.834dB

From the table I, it can be concluded that for 2.4GHz frequency at 0.18 um technology, compared to other LNAs, the designed LNA has least noise figure (of value 0.834 dB) and with a good value of gain (24.25 dB). So, our designed LNA, in terms of gain and noise, is much better as compared to other reported LNAs at 2.4 GHz

V. CONCLUSION

In this paper, a 2.4GHz CMOS LNA is proposed. Good noise figure value of 0.834 dB and high gain of 24.25 dB is achieved which shows that the proposed circuit has good stability, as obtained at 1.8V power supply.

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