1T DRAM Memory cell Design and analysis in CNTFET Technology

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Abstract— **In this paper, 1-Transistor DRAM cell has designed using the Carbon Nano-tube Field Effect Transistors (CNTFETs). Simulation of 1T DRAM cells using the Synopsys EDA tool (HSPICE) in 32nm technology analysis in terms of leakage current, leakage power, dynamic power dissipation, and average power has been done. And, also comparison has taken with 3T DRAM using CNTFET Transistor and shown 1TDRAM cells has advantaged over 3T DRAM cells, the size of 1TDRAM cells also reduce very much compare to other DRAM cells due to using of less number of transistor which is looking for the future requirement.**

Keywords— *Carbon Nano-tube FET (CNTFET), Three-transistor (3T),One-transistor(1T),dynamic random access memory(DRAM), n-type CNT.*

I. INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) has identified Carbon-based nanotechnology is one among seven "Beyond CMOS" for accelerated development in future innovations [1]. Dynamic random access memory (DRAM) integrated circuits (ICs) have existed for more than twenty-five years. DRAMs evolved from the earliest 1-kilobit (Kb) generation to the recent 1-gigabit (Gb) generation through advances in both semiconductor process and circuit design technology. Tremendous advances in process technology have dramatically reduced feature size, permitting ever higher levels of integration. These increases in integration have been accompanied by major improvements in component yield to ensure that overall process solutions remain cost-effective and competitive[2].

Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1. Since capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory [3]. The main memory (the "RAM") in personal computers is dynamic RAM (DRAM). It is the RAM in laptop and workstation computers as well as some of the RAM of video game consoles[4],[5]. The advantage of DRAM is its structural simplicity: only one transistor and a capacitor are required per bit, compared to four or six transistors in SRAM. This allows DRAM to reach very high densities. Unlike flash memory, DRAM is volatile memory (cf. non-volatile memory), since it loses its data quickly when power is removed. The transistors and capacitors used are extremely small; billions can fit on a single memory chip. 1T DRAM is a different way of constructing the basic DRAM bit cell. 1T DRAM is a "capacitorless" bit cell design that stores data in the parasitic body capacitor that is an inherent part of silicon on insulator (SOI) transistors. Considered a nuisance in logic design, this floating body effect can be used for data storage. Although refresh is still required, reads are non-destructive; the stored charge causes a detectable shift in the threshold voltage of the transistor. There are several types of 1T DRAM memories: the commercialized Z-RAM from Innovative Silicon, the TTRAM from Renesas and the A-RAM from the UGR/CNRS consortium. Faster versions of 1T DRAM are sometimes called 1T-SRAM. The classic one-transistor/one-capacitor (1T/1C) DRAM cell is also sometimes referred to as "1T DRAM"[6].

 Dynamic RAMs are important class of semiconductor devices based on the MOSFET with huge range of applications to all computational devices. DRAM integrated circuits also obey the Moore's law and thus, there is an urgent need of new materials to address the problems related to higher data storage, smaller sizes, higher density of integration, lower power consumption, higher reliability, faster performance, etc[7]. And all these requirements have to be met at a low cost. One very important aspect of device scaling is the extremely reduced oxide thickness of MOSFETs[8]. A prospective solution to this issue is the use of electronic devices with channels made of a single carbon nanotube or a semiconductor nanowire. Carbon nanotubes are sheets of graphite layers (grapheme, a semi-metal) rolled into a tube [9]. Depending on the way the sheet is rolled up (its chirality) the CNT may be metallic or semiconducting. Interest in carbon nanotubes is driven by their electronic, optical, thermal, and mechanical properties[10].   Carbon Nanotubes (CNTs) have been

attracting much attention in recent years due to its small dimension, unusual geometry and their extraordinary electronic properties. A CNT is a graphene sheet rolled up to form a hollow cylinder. It can exhibit a metallic or a semiconducting behavior and can present different diameters (at nanometer range) depending on its chirality (angle of the atom arrangement along the tube). Carbon Nanotube Field Effect Transistors (CNFETs) are promising candidates to replace silicon CMOS due to its high performance; mainly a high current driving capability, tolerance to temperature drift, leakage currents avoidance and self assembled growth[11] . A CNFET is like a conventional MOSFET, except that its channel is made up of one or more CNTs, and that the source and drain interfaces may be Schottky contacts.

A single-wall carbon nanotube (SWCNT) is a tube formed by rolling a single sheet of graphene. It can either be metallic or semiconducting depends on the chirality vector (m, n), i.e. the direction in that the graphene sheet is rolled. For CNFETs, the threshold voltage of the transistor is defined by the diameter of the carbon nanotubes, which is related to the chirality vector as follows:

$$D_{CNT} = \frac{a}{\pi}\sqrt{m^2 + n^2 + mn} \qquad (1)$$

$$V_{TH} = \frac{aV_\pi}{\sqrt{3} * qD_{CNT}} \qquad (2)$$

where q is the charge of a n electron, a = 2.49Å is the CNT atomic distance and V_π = 3.033eV is the carbon π to π bond energy[12]. The sizing of a CNFET is equivalent to adjusting the number of tubes.
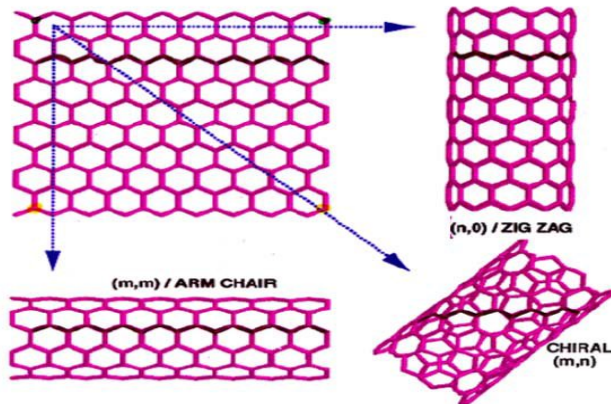

Figure 1: Structure of CNT based on chiral vector.

Since the mobility of n-type and the mobility of p-type carriers inside CNTs are identical, the minimum size is 1 for both P-CNFET and N-CNFET. The differences in the chiral angle and the diameter cause the differences in the properties

of the various carbon nanotubes[13]. For examples, it can be shown thatan (m ,n) carbon nanotube is metallic when m = n, has a small gap (i.e. semi-metallic) when n − m = 3i, where i is an integer, and is semiconducting when n − m ≠ 3i. This is due to the fact that the periodic boundary conditions for the one-dimensional carbon nanotubes permit only a few wave vectors to exist around the circumference of carbon nanotubes. Metallic conduction occurs when one of these wave vectors passes through the K-point of graphene's 2D hexagonal Brillouin zone, where the valence and conduction bands are degenerate [14].

II. 1TDRAM OPERATION

The circuit diagram of the one-transistor (1-T) DRAM cell consisting of one explicit storage capacitor and one access transistor is shown in Fig.2. Here, Cl represents the storage capacitor which typically has a value of 30 to 100 fF. Similar to the 3-T DRAM cell, binary data are stored as the presence or absence of charge in the storage capacitor. Capacitor *C2* represents the much larger parasitic column capacitance associated with the word line. Charge sharing between this large capacitance and the very small storage capacitance plays a very important role in the operation of the -T DRAM cell [15].
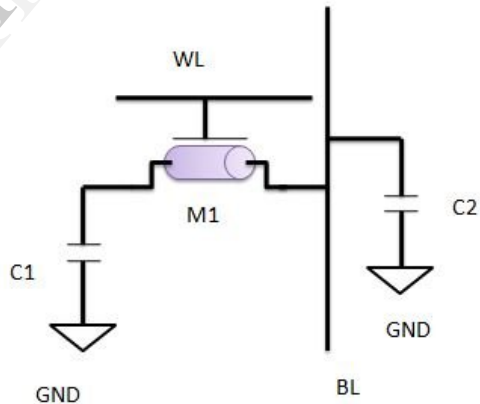

Figure 2: 1TDRAM Memory cell.

The "data write" operation on the 1-T cell is quite straightforward. For the write "1" operation, the bit line (BL) is raised to logic " 1 " by the write circuitry, while the selected word line is pulled high by the row address decoder. The access transistor Ml turns on, allowing the storage capacitor C to charge up to a logic-high level.

For the write "1" operation, the *inverse* data input is at the logic-low level, because the data to be written onto the DRAM cell is logic "1." Consequently, the "data write"

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transistor MD is turned off, and the voltage level on column *Din* remains high. Now, the "write select" signal WS is pulled high during the active phase of 02. As a result, the write access transistor Ml is turned on. With Ml conducting, the charge on *C2* is now shared with Cl (Fig.2). Since the capacitance C2 is very large compared to C1, the storage node capacitance Cl attains approximately the same logic-high level as the column capacitance C2 at the end of the charge-sharing process. Figure2. Charge sharing between *C2* and Cl during the write "I "sequence.

For the write "O" operation, the inverse data input is at the logic-high level, because the data to be written onto the DRAM cell is logic "0." Consequently, the data write transistor is turned on, and the voltage level on column Din is pulled to logic "0." Now, the "write select" signal WS is pulled high during the active phase of *02*. As a result, the write access transistor Ml is turned on. The voltage level on C2, as well as that on the storage node Cl, is pulled to logic "0" through MI and the data write transistor, as shown in Fig. 2. Thus, at the end of the write "0" sequence, the storage capacitance C1 contains a very low charge, and the transistor M2 is turned off since its gate voltage is approximately equal to zero. The bit line (BL) is pulled to logic "" and the word line is pulled high by the row address decoder. In this case, the storage capacitor C discharges through the' access transistor, resulting in a stored "" bit.

In order to read stored data out of a -T DRAM cell, on the other hand, we have to build a fairly elaborate read-refresh circuit. The reason for this is the fact that the "data read" operation on the one-transistor DRAM cell is by necessity a "destructive readout." This means that the stored data must be destroyed or lost during the read operation. Typically, the read operation starts with precharging the column capacitance *C.* Then, 'the word line is pulled high in order to activate the access transistor Ml. Charge sharing between C and *C* occurs and, depending on the amount of stored charge on *C,* the column voltage either increases or decreases slightly. Note that charge sharing inevitably destroys the stored charge on C. Hence, we also have to *refresh* data every time we perform a "data read" operation.

For "Read 1" operation, with the storage capacitance C charged-up to a logic-high level, transistor M1 is now conducting. In order to read this stored "1," the "read select" signal RS must be pulled high during the active phase of 02*,* following a pre-charge cycle. As the read access transistor M1 turns on, C1 and BL create a conducting path between the "data read" column capacitance *C1* and the ground. The capacitance *C1* charges through M1, and the rising column voltage is interpreted by the "data read" circuitry as a stored logic "1."

For read this stored "0," the "read select" signal RS must be pulled high during the active phase of *02,* following a pre-charge cycle. The word access transistor M1 turns on, there is conducting path between the column capacitance *C2*

and the ground (Fig.2). Consequently, *C2* does not discharge, but C1 is charge and the logic-high level on the column is interpreted by the data read circuitry as a stored "0" bit.

III. CNFET DRAM PERFORMANCE

HSPICE simulations have been performed using a Berkeley 32-nm PTM HP model and CNTFETs parameter models by Stanford University's Nanoelectronics Group. HSPICE is the most accurate circuit simulation that is used in much semiconductor industry setting[16]-[18]. The nominal charity of the CNTs is (19,0) and a pitch of 30nm,the length of doped CNT source/drain extension region (L_sd) = 32.0nm,Fermi level of the doped S/D tube (Efo) = 0.6 eV the thickness of high-k top gate dielectric material (Tox) = 4.0nm, Flatband voltage for n-CNTFET (Vfbn) = 0.0eV ,the mean free path in intrinsic CNT (Lceff) = 200.0nm, the mean free path in p+/n+ doped CNT = 15.0nm,the work function of Source/Drain metal contact = 4.6eV CNT work function = 4.5eV.

IV. SIMULATION AND ANALYSIS RESULT

We have simulated read and write operation of 1T and 3T(not included in paper) NCNTFET DRAM cells . Simulation of read and write operation of two transistor DRAM cell is successfully done. The simulations assume DRAM memory with 1T cells and 3T cells to evaluate performance with significant capacitive loading on the bit lines. The number of CNTs per transistor for 3T DRAM cell are M1 (5), M2 (5) both as precharge transistor, M3 (3), M5 (3) as pass transistor, M4 (3) as storage transistor and M6 (3) as data input transistor. The number of CNTs per transistor for the 1T cell is M1 (5), M2(3),and M3(3, where M1 has precharge transistor, M2 has pass transistor and M3 has data input transistor. The number of CNTs per transistor is set to be optimizing DRAM cell performance and functionality. The operation for both 1T DRAM cells and 3T DRAM cells are same, in these paper explained 1T DRAM cells only and four different operations for both cells are included below.
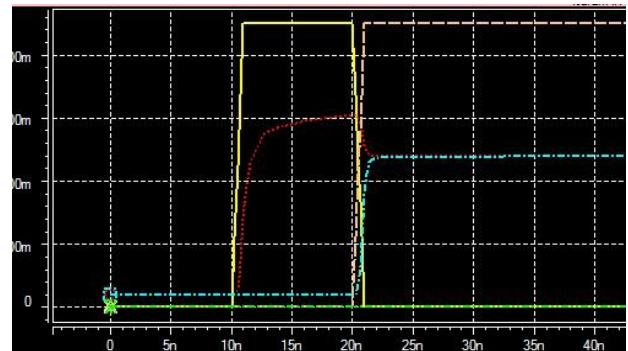

Figure 3: Waveform of "Write 1" operation in 1TDRAM cell.

When the precharge transistor is "ON", the C2 capacitance in bit line has fully charge up to .65mv, then inverse input data has apply, M3 transistor is still open stage. The charge from C2 to C1 has transferred when M1 has switch ON. The charging of C1 has depend on C2 and the number of tubes in

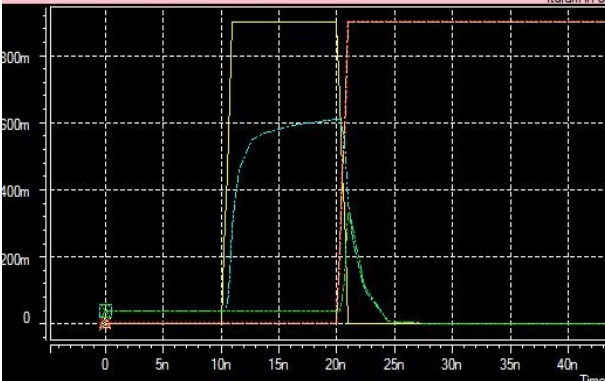transistor M1, in 1TDRAM has C2 has 30ff to 100ff capacitance (fig. 3).

Figure 4: Waveform of "Write 0" operation in 1TDRAM cell.

From the above waveform (fig. 4) has shown the "Write 0" operation because of inverse input data apply to the input transistor M3, the storage charge in Bit line has discharge to ground by making path through C2 to M3 then Ground . So, the C1 capacitance has not able to charge even the pass transistor is switch ON.
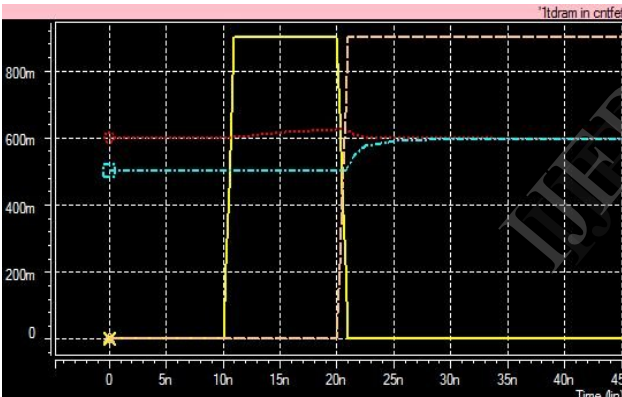

Figure 5: Waveform of "Read 1" operation in 1TDRAM cell.

From the above Fig. 5, has given the "Read 1" operation in 1TDRAM memory cell, when "Write 1" operation C1 has store charge i.e. initial condition of C1 has charge upto .5mv, the pass transistor has able to pass charge from C2 to the C1 that makes C1 has re-charge again .
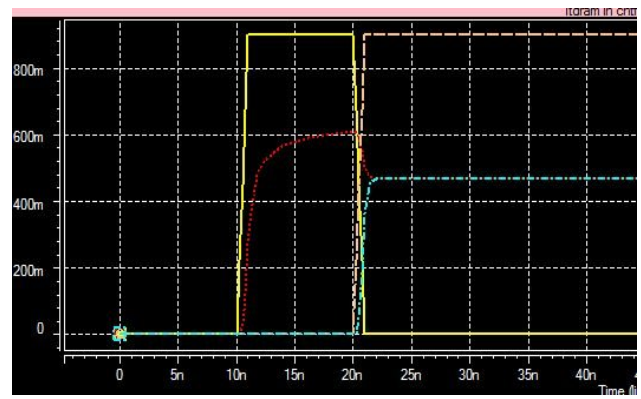

Figure 6: Waveform of "Read 0" operation in 1TDRAM cell.

The above fig. 6 has determined the "Read 0" operation in 1TDRAM cell, here the initial condition of the C1 (storage capacitor) has zero, because of pre-charging the bit lint Capacitor C2 has transferred to the C1 capacitor when Word line has high from low.
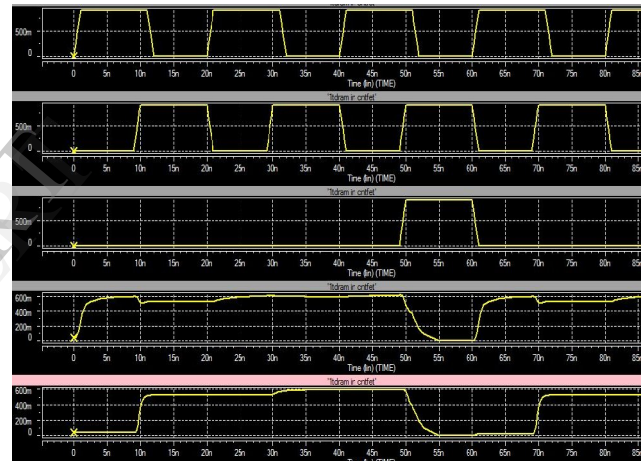

Figure 7: Waveform of "Write & Read" operation of 1TDRAM cell.

From fig. 7, has shown the overall of "Write" and " Read" operation of 1TDRAM Memory cells , first pulse has the required pre-charge pulse has been done for every read or write operation in the cell. Notably, all the operation has done during the pre-charge has low state.

The analysis result of the 1TDRAM Cell and 3TDRAM cell has given in the below tables, and also done the comparisons of both has taken place. The analysis parameters are leakage current in two states like "1" and "0", leakage power , dynamic power dissipation and average power dissipation has done in both 1TDRAM NCNFET and 3TDRAM NCNFET cells .

Results for NCNFET DRAM cells designed in this project Vdatain from time 0 to 90e-009:

TABLE 1: LEAKAGE POWER FOR DRAM cells.

Leakage pow. 1	1TDRAM	3TDRAM
Write 0	36nw	31nw
Read 0	37nw	31nw
Write 1	36nw	31nw
Read 1	20nw	31nw

TABLE 2: LEAKAGE POWER FOR DRAM cells.

Leakage pow. 0	1TDRAM	3TDRAM
Write 0	7nw	12uw
Read 0	13nw	12uw
Write 1	13nw	12uw
Read 1	14nw	13uw

TABLE 3: LEAKAGE CURRENT FOR DRAM cells

Leak.Current 1	1TDRAM	3TDRAM
Write 0	4.1077E-17A	3.4776E-17A
Read 0	4.210E-17A	3.4769E-17A
Write 1	4.104E-17A	1.9071E-18A
Read 1	2.2610E-17A	3.4683E-17A

TABLE 4: LEAKAGE CURRENT FOR DRAM cells

Leak Current 0	1TDRAM	3TDRAM
Write 0	7.8066E-19A	1.3574E-14A
Read 0	1.536E-20A	1.3574E-14A
Write 1	1.538E-20A	1.3574E-14A
Read 1	1.5613E-20A	1.4178E-14A

TABLE 5: AVERAGE POWER DISSIPATION FOR 1TDRAM CELL.

Avg. Dissipation	1TDRAM	3TDRAM
Write 0	59nw	81nw
Read 0	66nw	81nw
Write 1	59nw	81nw
Read 1	27nw	85nw

TABLE 6: DYNAMIC POWER FOR 4TDRAM.

Dyn.Dissipation	1TDRAM	3TDRAM
Write 0	58nw	81.7nw
Read 0	66nw	81.7nw
Write 1	58nw	81.5nw
Read 1	26nw	85nw

In leakage current and power 1TDRAM cell has more than 3TDRAM cell due to the using of large size of capacitance in storage as well as bit line capacitors, even this also in terms of the negligible value of powers shown in table 1& 2, the highest leakage power is 37nw in read 0 operation in 1TDRAM cells and also minimum leakage power is 20nw in 1TDRAM cell, but 3TDRAM cell has 13nw in all operations. The average power dissipation in 1TDRAM has maximum value of 66nw in read 0 operation and minimum of 27nw in read 1 operation ,even these values are still lower compare to 3TDRAM cells. Dynamic power dissipation in both cells has nearly equal to their respective values in average power dissipation because in CNFET transistor has minimized the static power dissipation in the memory cells.

V. CONCLUSIONS

In this paper, we have presented the 1TDRAM memory cell design with n-type metallic CNTs transistors using 32nm technology. The four operation of DRAM like "write 1" "write 0" "read 1" and "read 0" has done in the different waveform and the analysis of the leakage power, dynamic power dissipation and average power dissipation are taken using the HSPICE , a family of Synopsys EDA tools . and also comparisons of 3TDRAM CNFET memory cells also taken place and proof that 1TDRAM CNFET memory cell has better performance compare to the 3TDRAM CNFET memory cells in terms of power dissipation.

REFERENCES

[1] Zhe Zhang,"Carbon nano tube SRAM design with Metallic CNT or Removed Metallic CNT Tolerant Approaches" IEEE Trans. on Nanotechnology, vol. 11, pp. 788-798, July 2012.
[2] Balwant Raj, Anita Suman, and Gurmohan Singh, "Analysis of power dissipation in DRAM cells design for nanoscale memories," International journal of information technology and Knowledge Management, vol. 2, No. 2, pp. July/dec. 2009.
[3] P. L. McEuen, M. S. Fuhrer, and Park Hongkun, "Single-walled carbon nanotubeelectronics," IEEE Trans. on Nanotechnology, Vol. 1, No.1, pp. 78-85,2002.
[4] R. Saito, G. Dresselhaus, and M. Dresselhaus, "Physical Properties of Carbon Nanotubes," Impreial College Press, 1998.
[5] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," Applied Physics Letters, Vol. 73, pp. 2447-2449, 1998.
[6] Desmond C.Y.Chek, Michael L.P. Tan, Mohammad Taghi Ahmadi, and Razali Ismail, "Analytical modeling of high performance single-walled carbon nanotube field-effect-transistor",ELSEVIER Microelectronics Journal 41 (2010) pp. 579-584.
[7] J.Deng and H.-S.P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including non- idealities and its

application," IEEE Trans. Electron Devices, vol. 54, no. 12 , pp. 3195 – 3205, Dec. 2007 .

[8] Övünç Polat and Ali Manzak,"Evaluation of Low Power Carbon Nanotube Field Effect Transistor (CNTFET) Master-Slave Latches," in Proc.2012 ICICA,IPCSIT vol.32. 2008, pp.1543-1551.

[9] Alan C.Seabaugh,"Low-voltage Tunnel transistors for Beyond CMOS logic"Proceedings of IEEE , vol. 98, pp. 2095-2110, Dec.. 2010.

[10] Jae-yoon Sim, " Circuit Design of DRAM for Mobile Generation," Journal of semiconductor technology and science, vol. 7, No.1, March,2007.

[11] Mariya Lyubomirova Spasova, George Vasilev Angelov and Marin Hristov Hristov, "Simulation of 1T DRAM memory cell with Verilog-A Model of CNTFET in Cadence," Annual Journal of Electronics, 2012, ISSN 1314-0078.

[12] Rajendra Prasad, B.K. Madhavi, and K.Lal Kishore, " Design of low Write-power consumption SRAM cell based on CNTFET at 32nm technology," International Journal of VLSI design & Communication Systems(VLSICS), Vol.2, No.4, Dec.2011.

[13] Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design," 3rd Ed. New York: McGraw-Hill, 2003, ch. 10.

[14] Albert Malvino, David J Bates, "Electronic Principles," seventh edition. New delhi: Tata McGraw Hill Edication Private limited.2007.ch.7, 14.

[15] Neil H.E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design, a circuits and systems perspective," Third Edition. Dorling Kindersley(India) Pvt. Ltd.,2007

[16] International Technology Roadmap for Semiconductors.(2010).[Online]. Available: http://www.itrs.net/.

[17] Berkeley Predictive Technology Model. (2011). [Online]. Availability: http://www.ead.asu.edu./ptm/.

[18] CNTFET Models.(2011). [Online] .Availabile:http://nano.stanford.edu/models.

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