0.8 V Low Power Operational Transconductance Amplifier

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Abstract

This paper proposed an operational transconductance amplifier consumes low power and work at low voltage by operating the transistor in subthreshold region and designed in a area efficient 180nm CMOS technology. Rail to rail input operation is achieved by complementary input pairs. The DC open loop gain is 46.3 dB; unity gain frequency is 403.1 kHz with 87.67° phase margin. Slew-rate enhance by adaptive bias circuit is 0.105 V/µs with 10 pF capacitive loads. To increase CMRR of an op amp, a common-mode feed-forward circuit is used, keeping the DC gain almost constant. The proposed Op-Amp consumes less than 6µW at 0.8 V supply. Layout of an amplifier designed having an area of 78.39 µm x 40.82 µm.

1. Introduction

Low power circuit design is becomes very essential to fulfil the requirement for long-life portable devices. For less power consumption of analog circuits in active operation, the transistors operating in subthreshold region dissipate less leakage power than higher voltage alternatives [1]. In energy-constrained applications, conserving energy is the major goal and speed and dynamic range sometimes might have to be sacrificed, hence performance achieved in the sub-threshold region is more than adequate [2].

Active elements like operational transconductance amplifiers (OTA) are mostly used in application such as data converter, sensors, signal processors, etc [3]. With low voltage and power efficient operation, these OTA has to maintain slew rate without limiting the fast settling response. To address the above, this paper presents a CMOS operational transconductance amplifier targeting ultra low-power and low voltage applications. The main features are: sub-threshold operation, class AB operation, adaptive biasing and enhanced slew-rate (0.105 V/µs), ultra low-power consumption (~ 6µW), low voltage operation (0.8 V supply).

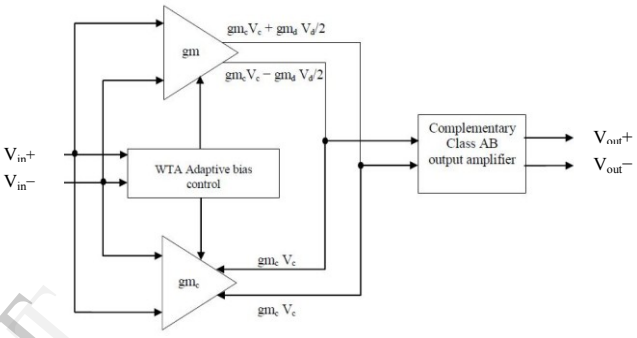


Fig. 1. Proposed operational transconductance amplifier

2. Operational Transconductance Amplifier

Figure 1 shows conceptual blocks of the proposed OTA. It made up of two main parts: one is the core of an amplifier formed with class AB output stage, and another is CMFF circuit; both are composed of adaptive bias and complementary input pairs.

The OTA has operating principle as: the input signals $V_{in}+/- = V_c \pm V_d/2$ where V_c is the common-mode input voltage and V_d is the differential input voltage, and because of rail to rail input operation V_d and V_c are converted into output currents I_o+ and I_o-.

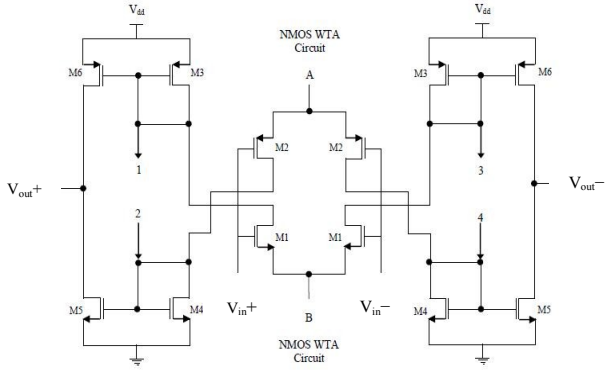


Fig. 2. Core of operational transconductance amplifier

Proposed OTA's most important parameter is transconductance (gm) contained two factors related to V_d and V_c are: differential gm (gm_d) and common mode gm (gm_c), respectively. Adding the sufficient extra current by CMFF circuit, the dependence of the output currents I_o+ and I_o- on V_c is removed. Irrespective of variations in the input common-mode voltage V_c, to keep DC voltage gain almost constant CMFF circuit biases conveniently the output stage of an OTA.

2.1. Rail to Rail Input Stage

Rail to rail input operation is achieved by complementary differential input pairs shown in fig. 2, as for high common mode input voltages NMOS differential pair is work and for low common mode input voltages PMOS differential pair is work. A common-mode input range which extends from rail to rail can be achieved by placing an n-channel and a p-channel input pair in parallel, rail to rail extension to common mode input voltage from rail is achieved [4]. For low voltage and power efficient operation, both NMOS and PMOS input transistors (M1 and M2 respectively) operate in sub-threshold.

2.2. Adaptive Bias Circuit

Adaptive bias circuit is used to overcome the issues like low-voltage, power-efficient operation and relatively high slew-rate, because the maximum output current is limited by bias current. Achieving large output current becomes more challenging in sub-threshold operation where bias currents are normally quite small. Adaptive bias circuits eventually boost dynamic currents when a large differential input signal is applied, keeping maximum current levels well above the quiescent currents. These quiescent currents can be made very low to reduce static power dissipation by operating transistors in subthreshold region.

To achieve enhanced slew-rate, Winner-Take-All (WTA) circuit is used as adaptive biasing technique [5]. Input differential pair PMOS and NMOS are biased by PMOS and NMOS WTA circuits shown in Fig. 3(a) and 3(b), respectively are employed. Transistors M7, M8, M11 and M12 are operate in sub-threshold while transistors M9 and M10 operate in strong inversion while. Because output of each WTA circuit is the maximum of the input voltages, the common-source node voltage of the differential pair is maximum input voltage shifted by $V_{GSM8(11)}$ voltage, which determines the main pair quiescent currents (~266nA for V_c = 0.4 V). If for instance input voltage $V_{in}+$ increases and becomes higher than $V_{in}-$, then source node will track $V_{in}+$ and increases source voltage of input pairs, consequently, modifying the currents flowing through them. Thus, the dynamic currents can be much larger than the quiescent current.

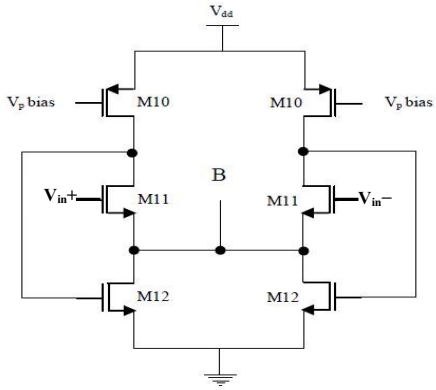
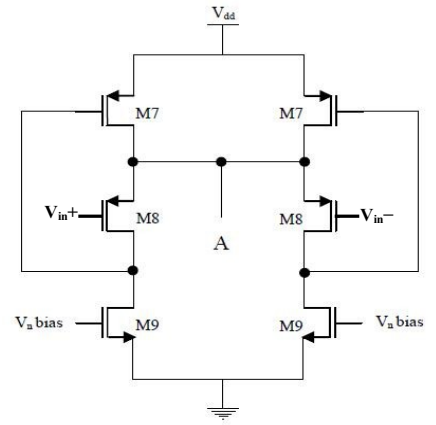


Fig. 3. (a) NMOS WTA



(a) PMOS WTA

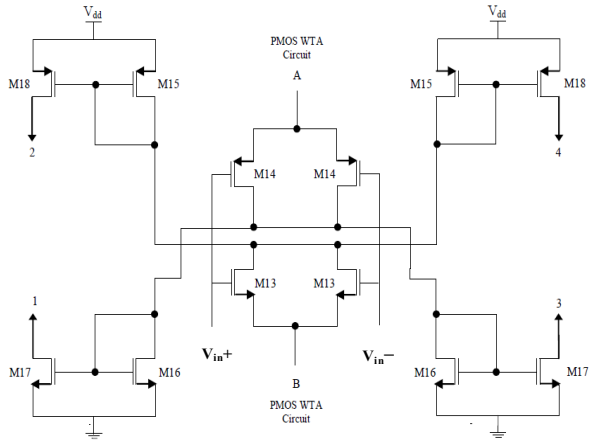


Fig. 4. Common Mode Feed Forward Circuit

2.3. Common Mode Feed Forward

To reject input signals common to both inputs, high CMRR is essential as in every fully differential operational transconductance amplifier. Normally, common-mode feedback (CMFB) or/and feed forward (CMFF) circuits are assigned to achieve high CMRR.
The CMFF approach improves the induced nonlinear distortion, output signal swing and even the frequency response of the system so comparative studies among CMFB and CMFF techniques for LV applications shows CMFF technique is best suitable [6].
As said earlier, CMFF has two purposes: firstly, it conveniently biases low voltage rail-to-rail outputs so that in spite of variations in the supply voltage, process and V_c, output common mode voltage Vo_c remains almost constant and secondly, it removes the dependence of output currents I_o^+ and I_o^- on the input common-mode voltage V_c (fig. 1). The output stage in fig. 2 can be shown in DC by removing CMFF circuit shown in fig. 5, as transistors M3 and M4 biased the a CMOS current source (M6) and a current sink (M5) connected in series. In this figure, the DC currents that flow by the each of NMOS and PMOS that is by input transistors M1 and M2 are I_N and I_P. The largest current carrying transistor forcefully enters into the triode region, since smallest current dominates and makes $I_6 = I_5 = \min(I_6, I_5)$. Consequently, if the DC current that carries the current source PMOS and the current sink NMOS are always the same then both transistors will be kept in saturation.
In this way, some complementary DC current I_3' and I_4' has to be added to $I_3 = I_N$ and $I_4 = I_P$, to make $I_3 = I_4$. A better way is to make $I_3' = I_P$ and $I_4' = I_N$ and in this case, the tail currents of the input pairs are summation of $I_3 = I_4 = I_N + I_P$. The, generated by transistors M13-M15 and M14-M16 generate the currents I_3' and I_4', which are added to the core of the OTA, by means of the transistors M17 and M18, respectively. All the transistors operate in sub-threshold region in quiescent conditions.

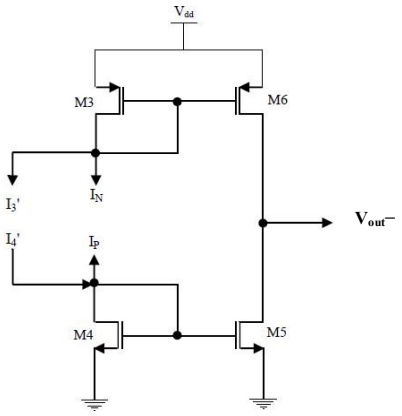


Fig. 5. Conceptual schematic of an output stage for DC currents

3. Results And Analysis

The proposed OTA is designed in 180nm CMOS technology with 0.8 V power supply. Simulations are done using Cadence Virtuoso Spectre with a BSIM3v3.2 model for the GPDK 180nm CMOS technology. The DC open-loop gain of 46.31 dB is obtained as shown in fig. 7. Unity gain frequency of 407.1 kHz as depicted in fig. 7, with a phase margin of 87.67º is shown in fig. 8 are measured. The power consumption of the operational amplifier is nearly equal to 6µW. Slew-rate (SR) obtained in a non-inverting voltage follower configuration, with a capacitive load of 10 pF connected to the amplifier outputs is 0.105 V/µs shown in fig. 9. Common mode rejection ratio is 119.3dB as shown in fig. 10. And power supply rejection ratio of an OTA as shown in fig. 11 is 102 dB.
The layout of designed OTA is shown in fig. 12, designed with the help of state of art layout design techniques to prevent contribution of parasitic and is heavily area constrained. Designed layout has optimized area of 78.39 µm x 40.82 µm. Post layout simulation results are compared to that of with pre-layout simulations. And it is found that they are same and match. Table I summarized the performance of proposed OTA, compared with previously proposed

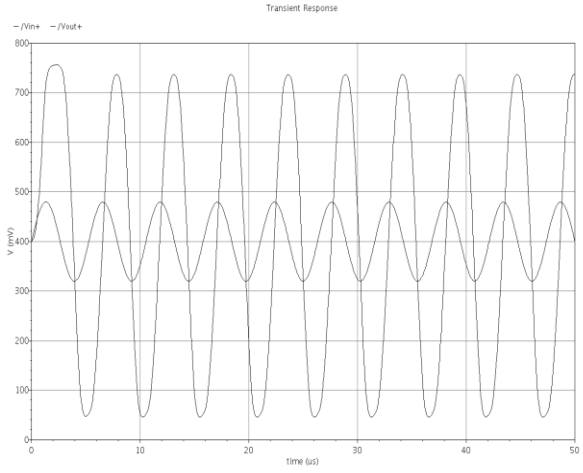


Fig. 6. Input and output swing

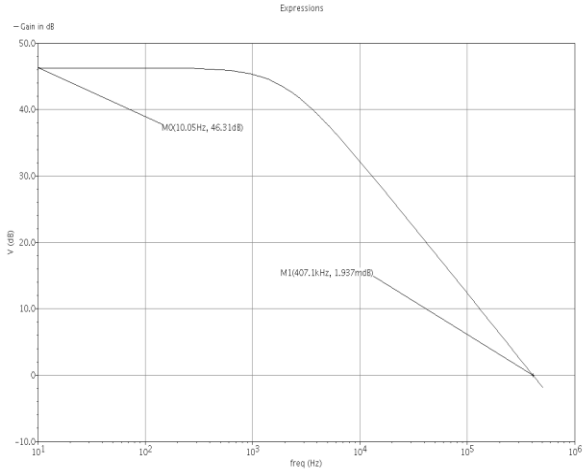


Fig. 7. OTA Gain

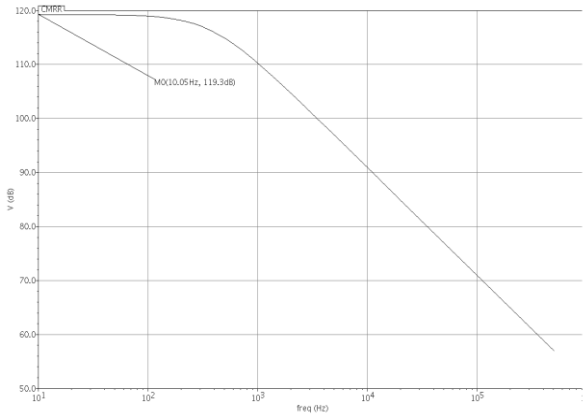


Fig. 10. CMRR

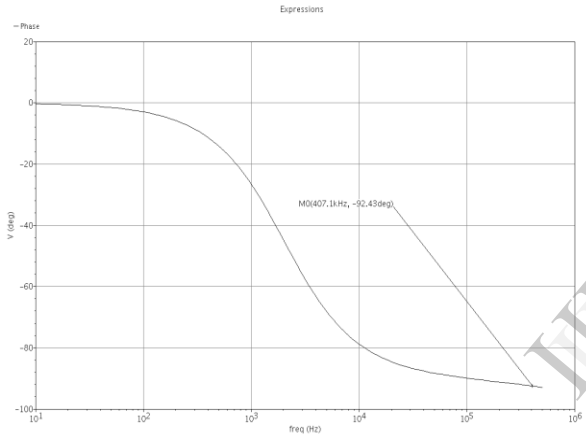


Fig. 8. Phase Margin of an OTA for 10pF load

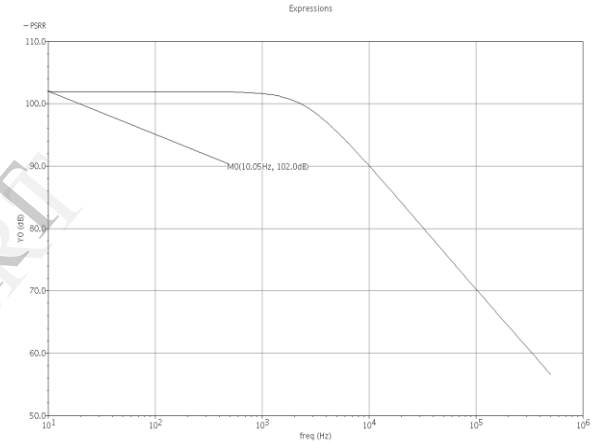


Fig. 11. PSRR

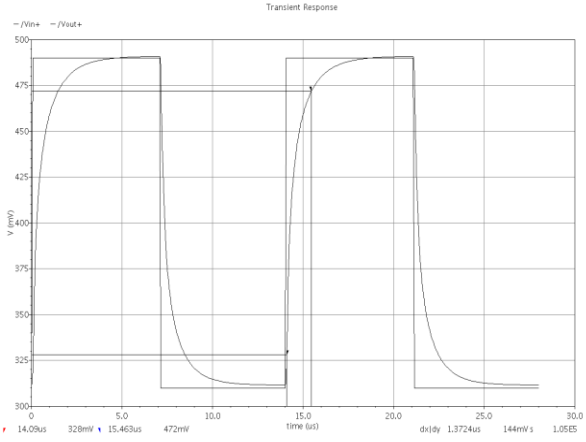


Fig. 9. Slew rate with 10pF capacitive load

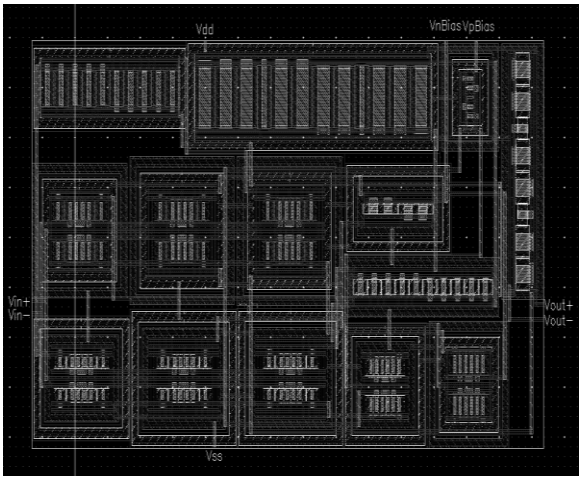


Fig. 12. Layout of an OTA

fully differential Op-Amp designs [1, 7-9]. As shown, this new OTA has a better bandwidth with good phase margin, achieving better performance parameter in terms of reduced power consumption, having good PSRR.

4. Conclusion

Operational transconductance amplifier having a subthreshold operation and compact design, immensely targeting growing demand towards low cost and battery operated portable devices is presented. A novel design adaptive bias technique and CMFF circuits are used to enhance the performance. A standard 180nm CMOS process is used to obtain desirable performance with very compressed supply voltage of 0.8V rather than conventional 1.8V. Layout designed is highly area constrained having rectangular area of 78.39 µm x 40.82 µm.

Table1. Comparison of fully differential amplifiers

Parameter	**[1]**	**[7]**	**[8]**	**[9]**	**This work**
Supply Voltage	0.8 V	0.5 V	0.8 V	0.8 V	0.8 V
Technology (CMOS)	180 nm	180 nm	180 nm	350 nm	180 nm
DC Gain	51 dB	55 dB	68 dB	66 dB	46.31 dB
Unity gain frequency	40 kHz (CL = 10pF)	8.72 MHz (CL = 10pF)	8.12 MHz (CL= 1pF)	3.4 MHz (CL= 5pF)	407.1 kHz (CL= 10pF)
Phase margin	65°	61°	89°	80°	87.67°
CMRR	65 dB	78 dB	–	–	119.3dB
PSRR	–	76 dB	–	–	102dB
Slew Rate	0.12 V/µs	2.92 V/µs	–	5.1 V/µs	0.105 V/µs
Power	1 µW	77 µW	94 µW	194 µW	6 µW

5. References

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