Current Mode Sense Amplifier for SRAM Memory

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Abstract

The sense amplifier is one of the most important components of semiconductor memories used to sense stored date. This plays an important role to reduce the overall sensing delay and voltage. Earlier voltage mode sense amplifiers are used to sense the date it sense the voltage difference at bit and bitb lines but as the memory size increase the bit line and date line capacitances increases. As a result large time is required by capacitance to discharge so sensing delay and power dissipation increase. Used that sense the current directly from bit and bitb lines and reduce the sensing delay. This technique is used in current mode sense amplifiers. This paper explores the design and analysis of current mode sense amplifier using Tanner tool (14.0) version. The simulation is carried out at 1.5V / 0.13um technology using tanner (14.0 Version) tool. The results are verified with the existing results at 1.8V / 0.18um CMOS technology.

1. Introduction

Sense Amplifier is the most critical circuit in the periphery of CMOS memory. The performance of SA's strongly affects both memory access time, and overall memory dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These objectives are somewhat conflicting when it comes to sense amplifier in memories. This increased bit-line capacitance in turn shows down voltage sensing and makes bit-line capacitance swings energy expensive resulting in slower more energy hungry memories. Due to their great importance in memory performance sense or detect stored data from a read-selected memory cell Sense amplifiers are used to translate small differential voltage to a full logic signal that can be further used by digital logic. The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for future sense amplifiers [6].

Moore's law was the breakthrough and evolution in the semiconductor industry. Moore's law gave the idea to integrate large memory blocks with logic circuits on a single chip but the on-chip memory limits the speed and performance of the overall system. The limiting factor is the increasing bit line capacitance, which results in increased time to develop bit line differential voltage and increase in the delay. For fast and power efficient memory design, both time and signal swing on the bit lines needs to be minimized. [4]

Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. Their performance strongly affects both memory access time, and overall memory power dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These objectives are somewhat conflicting when it comes to design the sense amplifier in memories. With increased memory capacity usually the bit-line parasitic capacitances get increased. This increased bit-line capacitance slows down voltage sensing and these results in slow and more power consuming memories.

Sense amplifiers are mainly used to read the contents of SRAM and DRAM cells. They are very sensitive to noise and their design implies that they will provide adequate noise margins and provide good quality of data that represent the contents of a particular memory cell. There are two categories of sense amplifiers. The static sense amplifiers mainly used to detect logic in the static RAMs and the dynamic sense amplifiers mainly used to save energy when low power dissipation is required. [9]

Fast sense amplifiers are important for achieving low latency in many circuits and the most common domain being bit-line reading in memories. With the advent of sub-micron CMOS chips, interconnection is becoming a major source of on-chip delay, and fast sense amplifiers are also likely to be needed, e.g. as repeaters for high-speed signals which must traverse large chips.

Sense amplifier can be operated in voltage, current and charge mode but we operate them in current-mode because they present a low impedance to the inputs and respond to the differential current rather than to the voltage between the inputs , this can reduce interconnect delay in long wires there by providing speed improvement. The current mode sense amplifier reduces and the low output resistance of the short-channel transistors

motivation to use current mode sensing in the bit lines in SRAM. [5]

The speed of the sensing operation depends on the ability of the sense amplifier as to how fast it can resolve or decide that which of the two bit lines current is higher in magnitude and accordingly provide a logic value of "1" or "0" in the output.

2. Current mode sense-amplifier circuit

The sense amplifier is selected by grounding the Ysel node as shown in fig-1. Then the currents will flow through the transistors via the bit-line loads. The drains of T3 and T4 are connected to data lines, which are close to ground level. This means that these transistors operate in saturation. The bit-line loads are low ohmic to ensure that the bit lines are always close to VDD during read access.

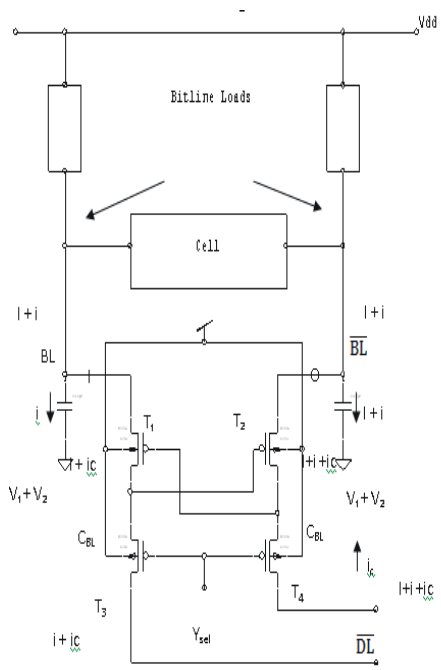

Figure-1 Current mode sense amplifier [1]

The sensing delay is unaffected by the bit-line capacitance since no differential capacitor discharging is required to sense the cell data.

The bit line swing during read operation as compared to voltage mode sensing technique. It proves that current

sensing technique would be faster than voltage mode due to the low impedance termination of the current mode. It shows that current sensing is relatively insensitive to the bit line capacitance.

The circuit operates as follows:-Suppose the cell is accessed and draws current I. The gate-source voltage of T1 will be equal to that of T3, since their currents are equal, their sizes are equal, and both transistors are in saturation. This voltage is represented by V1. The same applies to T2 and T4. Their gate-source voltages are represented by V2. It follows that, since Ysel is grounded, the left bit line will have voltage V1 + V2, and the right bit line will also have voltage V1 + V2. Therefore the potential of the bit lines will be equal independent of the current distribution. This means that there exists a virtual short circuit across the bit lines. Since the bit line voltages are equal, the bit-line load current will also be equal, as well as the bit-line capacitor currents. As the cell draws current Icell, it follows that the right-hand leg of the sense amplifier must pass more current than the left-hand leg. In fact, the difference between these currents is Icell (the cell current). The drain currents of T3 and T4 are passed to current transporting data lines DLs.

Sufficient margin from unwanted latching behavior is provided by the bit-line load resistance, the body effect, the differential data-line current is therefore equal to the cell current. Thus we obtain current sensing. The cross-coupled structure is actually a flip-flop configuration, but

A second speed-enhancing feature is provided by the common-mode discharge current pulses from the bit-line capacitors, effectively precharging the sense amplifier (in particular pre charging nodes A and B, and the data lines) as soon as Ysel is grounded. This is a kind of dynamic biasing which is very favourable for speed, and which does not increase the current consumption. Finally, since the bit-line voltages are kept equal, the sense amplifier possesses intrinsic equalizing action. This eliminates the need for bit-line equalization during a read access [1].

The analysis for conventional current mode Sense amplifier is done at TMSC 0.13um technology node with 1.5V power supply. The value of sensing delay is calculated for combinations of CBL = 1PF.

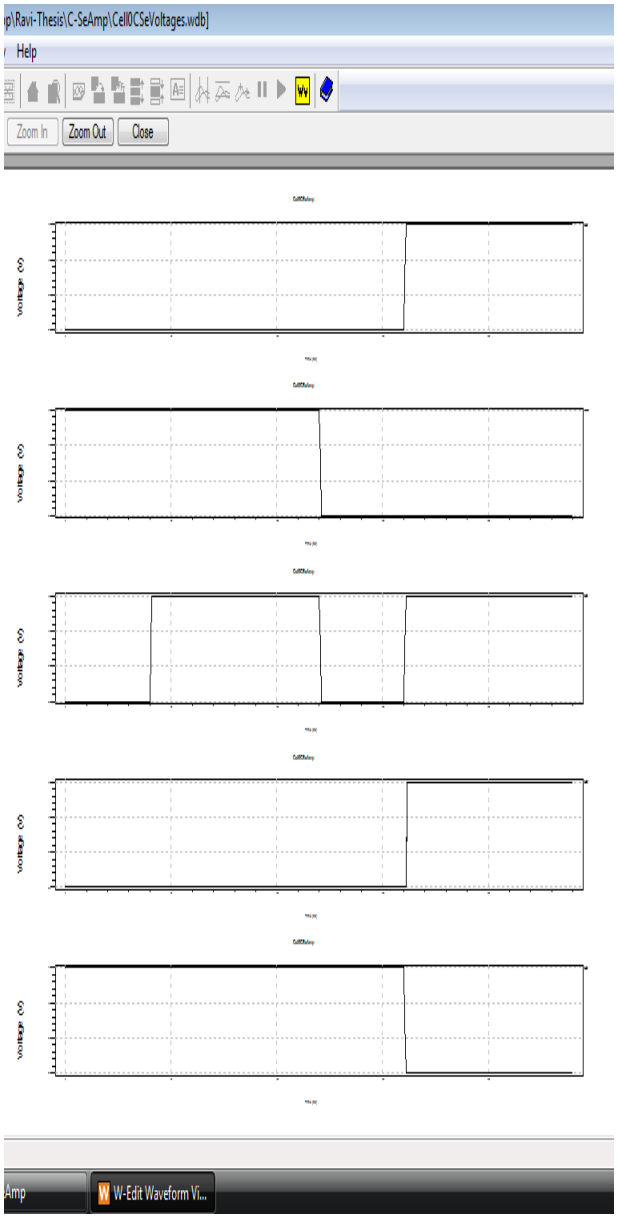

Figure-2 Voltage waveforms of current mode sense amplifier

Voltage Signal of Current Mode Sense Amplifier Circuit at Node-VS

Voltage Signal of Current Mode Sense Amplifier Circuit at Node-CLK

Voltage Signal of Current Mode Sense Amplifier Circuit at Node-WL

Voltage Signal of Current Mode Sense Amplifier Circuit at Node-Out

Voltage Signal of Current Mode Sense Amplifier Circuit at Node-CS

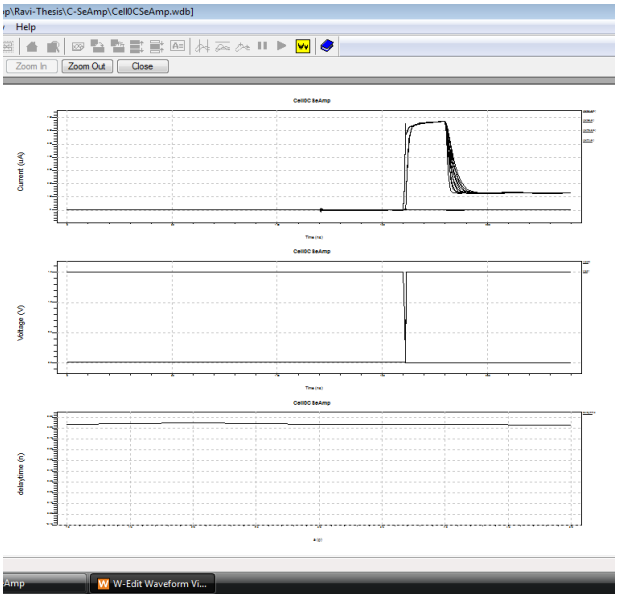

Figure-3 Simulation waveforms of conventional current mode sense amplifier circuit

Table-1 Comparison of sensing delay for current mode sense amplifier at CDL = 1PF, Cout = 0.1 PF and CBL varies from 1 Pf of 5 Pf

Bit Line Capacitance CBL(pf)	**Sensing Delay(ns)**
1	Measurement result summary - a=1e-012 Delay time = 8.3632e-010
2	Measurement result summary - a=2e-012 D delay time = 8.4438e-010
3	Measurement result summary - a=3e-012 Delay time = 8.3396e-010
4	Measurement result summary - a=4e-012 Delay time = 8.2980e-010
5	Measurement result summary - a=5e-012 Delay time = 8.2191e-010

The analysis for conventional current mode Sense amplifier is done at TMSC 0.13um technology node with 1.5V power supply. The value of sensing delay is calculated for combinations of CBL = 1PF,

CDL = 1PF Cout = 0.1Pf as shown in table-1.The analysis shows that the sensing speed of conventional current mode Sense amplifier independent of the variations in bit line capacitances.

3. Conclusion

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